FEATURES

- ï 5V Operation
- ï Full duplex asynchronous receiver and transmitter
- ï Easily interfaces to most popular micro-processors
- ï Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from a serial data stream
- ï Independently controlled transmitter, receiver, line status, and data set interrupts
- ï Programmable baud rate generator allows division of any input clock by 1 to (2^{16}-1) and generates the internal 16 x clock
- ï Independent receiver clock input
- ï MODEM control functions (CTS, RTS, DSR, DTR, RI,and DCD)
- ï Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, 1.5, or 2 stop bit generation
  - Baud generation (DC to 56k baud)
- ï False start bit detection
- ï Complete status reporting capabilities
- ï Tri-StateÆTTL drive capabilities for bi-directional data bus and control bus
- ï Line break generation and detection
- ï Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity overrun, and framing error simulation
- ï Fully prioritized interrupt systems controls
- ï 16 byte FIFO for reduced CPU overhead

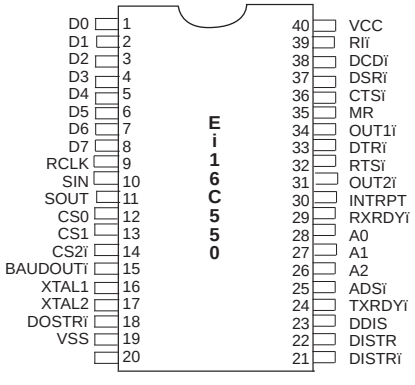
DESCRIPTION

The Epic Ei16C550 Universal Asynchronous Receiver Transmitter (UART) is a CMOS-VLSI communication device in a single package.

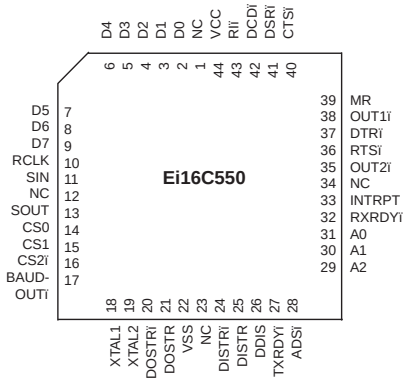
The UART performs serial to parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversions on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operation being performed by the UART, as well as any error conditions (party, overrun, framing, or break detect).

Part Numbers May Be Marked With "IMP" or "Ei."

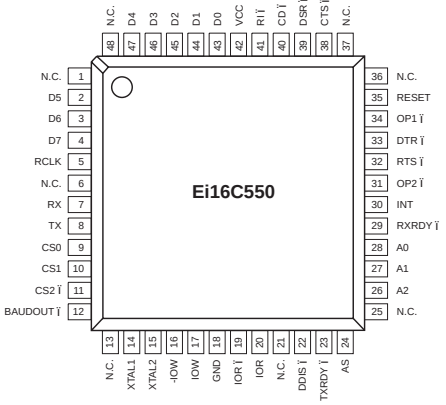
PIN CONFIGURATION



40-PIN DIP



44-PIN PLCC



48-PIN TQFP

The UART includes a programmable baud generator which is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1), and producing a 16 x clock to drive the receiver logic. Also included in the UART is a complete MODEM control capability, and processor interrupt system that may be software tailored to the users requirement to minimize the computing needed to handle the communications link.

BLOCK DIAGRAM