

# 128Mbit DDR SDRAM

***1M x 32Bit x 4 Banks  
Double Data Rate Synchronous DRAM  
with Bi-directional Data Strobe and DLL  
(144-Ball FBGA)***

**Revision 2.0**

**January 2003**

Samsung Electronics reserves the right to change products or specification without notice.

**Revision History****Revision 2.0 (January 16, 2002)**

- Changed package ball height from 0.25mm to 0.35mm
- Typo corrected

**Revision 1.9 (July 18, 2002)**

- Changed power dissipation from 2.0W to 2.3W

**Revision 1.8 (June 12, 2002)**

- Supported both CL4 and CL3 for the K4D263238A-GC45 and the effective date of this change starts from [WW23](#)

**Revision 1.6 (January 30, 2002)**

- Changed tCK(max) of K4D263238A-GC40 from 7ns to 10ns.
- Changed tCK(max) of K4D263238A-GC33/36 from 5ns to 4ns. **For all the CL5 operation, guaranteed tCK(max) is 4ns.**

**Revision 1.5 (December 14, 2001)**

- Removed K4D26323RA-GC2A/33/36(VDD/VDDQ=2.8V) & K4D263238A-GC55/60 from the spec.
- Added K4D263238A-GC36(VDD/VDDQ=2.5V)

**Revision 1.4 (November 14, 2001)**

- Added K4D26323RA-GC36(VDD/VDDQ=2.8V)

**Revision 1.3 (October 22, 2001)**

- Corrected part number of K4D263238A-GC2A to K4D26323RA-GC2A
- Changed tCDLR of -GC2A and GC33 from 3tCK to 2tCK and applied since Sept 15, 2001.
- Defined x32 DDR for mobile PC graphics separately - K4D26323AA-GL\*\* featured with VDDQ=1.8V, ICC6=1mA with reduced operating current. Refer to the K4D26323AA-GL\*\* spec for more detail information.

**Revision 1.2 (September 13, 2001)**

- Define DC spec value of K4D26323RA-GC33 and K4D263238A-GC2A
- Changed tCK(max) of -2A and -33 from 7ns to 5ns

**Revision 1.1 (September 3, 2001)**

- Added K4D26323RA-GC33(VDD/VDDQ=2.8V)
- Added K4D263238A-GC2A(350MHz)

**Revision 1.0 (August 16, 2001)**

- Changed tCDLR of K4D263238A-GC33 from 2tCK to 3tCK
- Removed VDDQ=1.8V from the spec.
- Added K4D263238A-GL as a low power part
- Defined DC spec.

**Revision 0.1 (August 2, 2001) - Target Spec**

- Changed tCK(max) of K4D263238A-GC45/-50/-55/-60 from 7ns to 10ns.

**Revision 0.0 (June, 2001) - Target Spec**

- Defined Target Specification

## **1M x 32Bit x 4 Banks Double Data Rate Synchronous DRAM with Bi-directional Data Strobe and DLL**

### **FEATURES**

- 2.5V  $\pm$  5% power supply for device operation
- 2.5V  $\pm$  5% power supply for I/O interface
- SSTL\_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
  - Read latency 3,4,5 (clock)
  - Burst length (2, 4, 8 and Full page)
  - Burst type (sequential & interleave)
- Full page burst length for sequential burst type only
- Start address of the full page burst should be even
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- No Write-Interrupted by Read Function
- 4 DQS's ( 1DQS / Byte )
- Data I/O transactions on both edges of Data strobe
- DLL aligns DQ and DQS transitions with Clock transition
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 32ms refresh period (4K cycle)
- 144-Ball FBGA
- Maximum clock frequency up to 300MHz
- Maximum data rate up to 600Mbps/pin

### **ORDERING INFORMATION**

Part NO.	Max Freq.	Max Data Rate	Interface	Package
K4D263238A-GC33	300MHz	600Mbps/pin	SSTL_2 (VDD/VDDQ=2.5V)	144-Ball FBGA
K4D263238A-GC36	275MHz	550Mbps/pin		
K4D263238A-GC40	250MHz	500Mbps/pin		
K4D263238A-GC45	222MHz	444Mbps/pin		
K4D263238A-GC50	200MHz	400Mbps/pin		

### **GENERAL DESCRIPTION**

#### **FOR 1M x 32Bit x 4 Bank DDR SDRAM**

The K4D263238A is 134,217,728 bits of hyper synchronous data rate Dynamic RAM organized as 4 x1,048,576 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 2.4GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

**PIN CONFIGURATION (Top View)**

	2	3	4	5	6	7	8	9	10	11	12	13
B	DQS0	DM0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	DM3	DQS3
C	DQ4	VDDQ	NC	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	NC	VDDQ	DQ27
D	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
E	DQ7	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ24
F	DQ17	DQ16	VDDQ	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	VDDQ	DQ15	DQ14
G	DQ19	DQ18	VDDQ	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	VDDQ	DQ13	DQ12
H	DQS2	DM2	NC	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	NC	DM1	DQS1
J	DQ21	DQ20	VDDQ	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	VDDQ	DQ11	DQ10
K	DQ22	DQ23	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ8
L	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	VDD	VSS	A10	VDD	VDD	RFU <sub>1</sub>	VSS	VDD	NC	NC
M	$\overline{\text{RAS}}$	NC	NC	BA1	A2	A11	A9	A5	RFU <sub>2</sub>	CK	$\overline{\text{CK}}$	MCL
N	$\overline{\text{CS}}$	NC	BA0	A0	A1	A3	A4	A6	A7	A8/AP	CKE	VREF

**NOTE:**

1. RFU1 is reserved for A12
2. RFU2 is reserved for BA2
3. VSS Thermal balls are optional

**PIN DESCRIPTION**

CK, $\overline{\text{CK}}$	Differential Clock Input	BA0, BA1	Bank Select Address
CKE	Clock Enable	A0 ~A11	Address Input
$\overline{\text{CS}}$	Chip Select	DQ0 ~ DQ31	Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe	VDD	Power
$\overline{\text{CAS}}$	Column Address Strobe	VSS	Ground
WE	Write Enable	VDDQ	Power for DQ's
DQS	Data Strobe	VSSQ	Ground for DQ's
DM	Data Mask	NC	No Connection
RFU	Reserved for Future Use	MCL	Must Connect Low

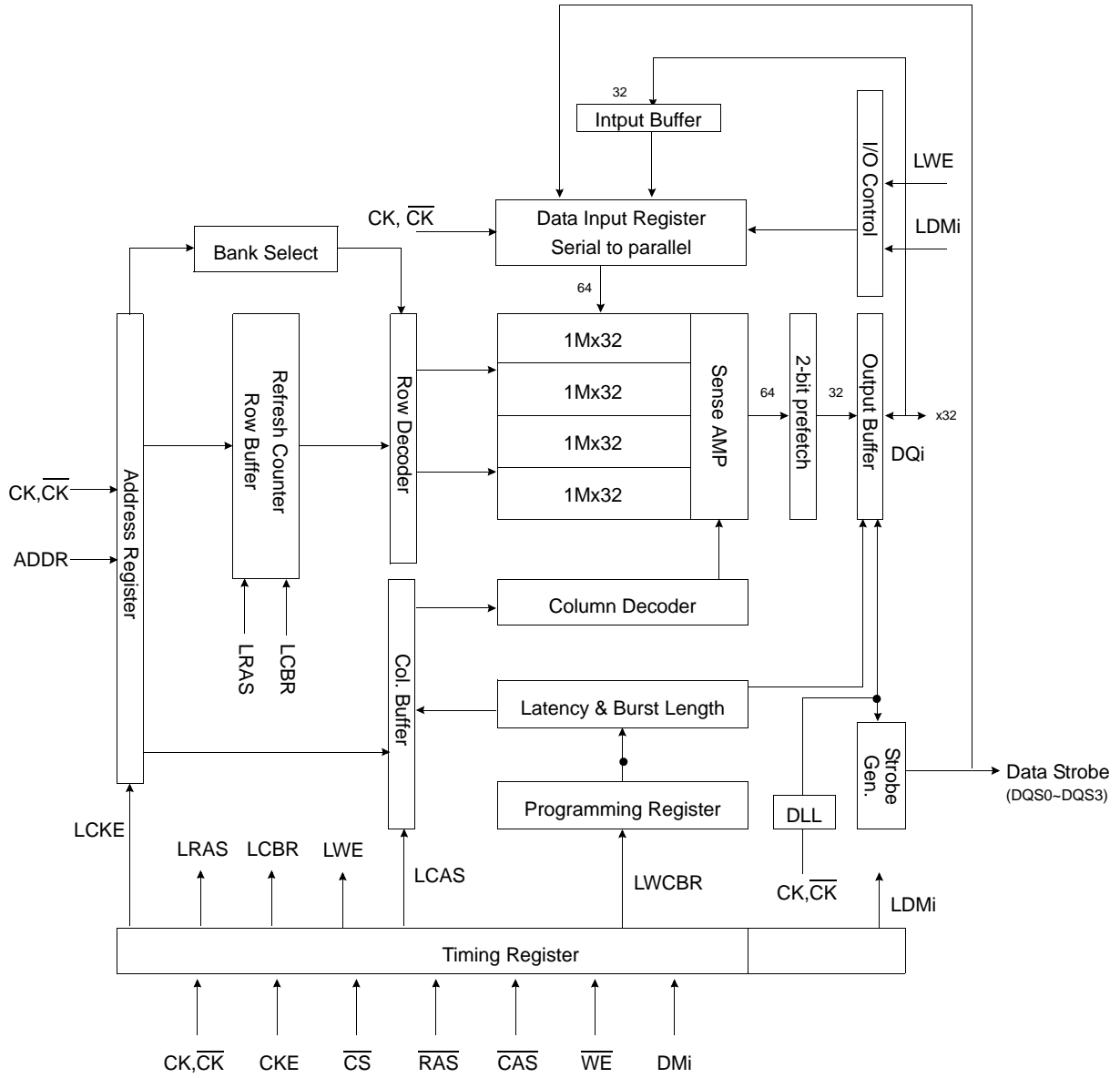
## INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, $\overline{CK}^{*1}$	Input	The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS.
CKE	Input	Activates the CK signal when high and deactivates the $\overline{CK}$ signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode.
$\overline{CS}$	Input	$\overline{CS}$ enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$	Input	Latches row addresses on the positive going edge of the CK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Input	Latches column addresses on the positive going edge of the CK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Input	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$ , $\overline{WE}$ active.
DQS0 ~ DQS3	Input/Output	Data input and output are synchronized with both edge of DQS. DQS0 for DQ0 ~ DQ7, DQS1 for DQ8 ~ DQ15, DQS2 for DQ16 ~ DQ23, DQS3 for DQ24 ~ DQ31.
DM0 ~ DM3	Input	Data In mask. Data In is masked by DM Latency=0 when DM is high in burst write. DM0 for DQ0 ~ DQ7, DM1 for DQ8 ~ DQ15, DM2 for DQ16 ~ DQ23, DM3 for DQ24 ~ DQ31.
DQ0 ~ DQ31	Input/Output	Data inputs/Outputs are multiplexed on the same pins.
BA0, BA1	Input	Selects which bank is to be active.
A0 ~ A11	Input	Row/Column addresses are multiplexed on the same pins. Row addresses : RA0 ~ RA11, Column addresses : CA0 ~ CA7. Column address CA8 is used for auto precharge.
VDD/VSS	Power Supply	Power and ground for the input buffers and core logic.
VDDQ/VSSQ	Power Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
VREF	Power Supply	Reference voltage for inputs, used for SSTL interface.
NC/RFU	No connection/ Reserved for future use	This pin is recommended to be left "No connection" on the device
MCL	Must Connect Low	Must connect low

\*1 : The timing reference point for the differential clocking is the cross point of CK and  $\overline{CK}$ .

For any applications using the single ended clocking, apply VREF to  $\overline{CK}$  pin.

BLOCK DIAGRAM (1Mbit x 32I/O x 4 Bank)



**FUNCTIONAL DESCRIPTION**

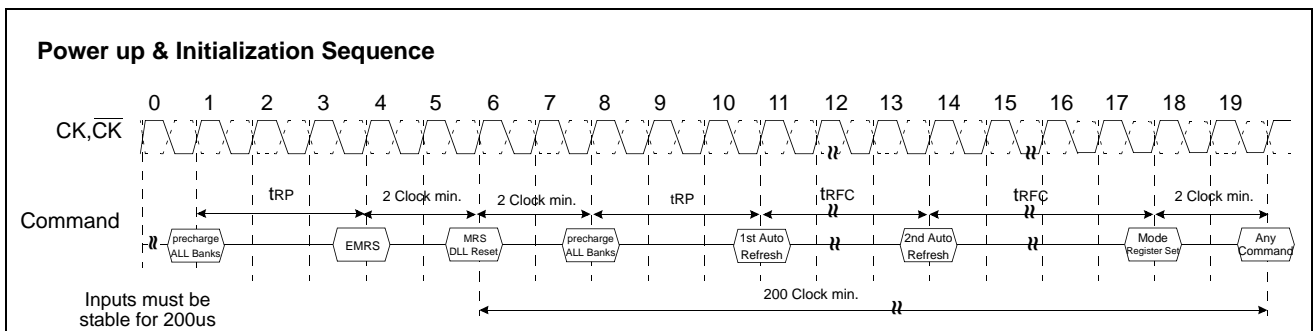
**• Power-Up Sequence**

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
  - Apply VDD before VDDQ .
  - Apply VDDQ before VREF & VTT
2. Start clock and maintain stable condition for minimum 200us.
3. The minimum of 200us after stable power and clock(CK,CK $\bar{}$ ), apply NOP and take CKE to be high .
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL
- \*1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.
- \*1,2 7. Issue precharge command for all banks of the device.
8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

\*1 The additional 200cycles of clock input is required to lock the DLL after enabling DLL.

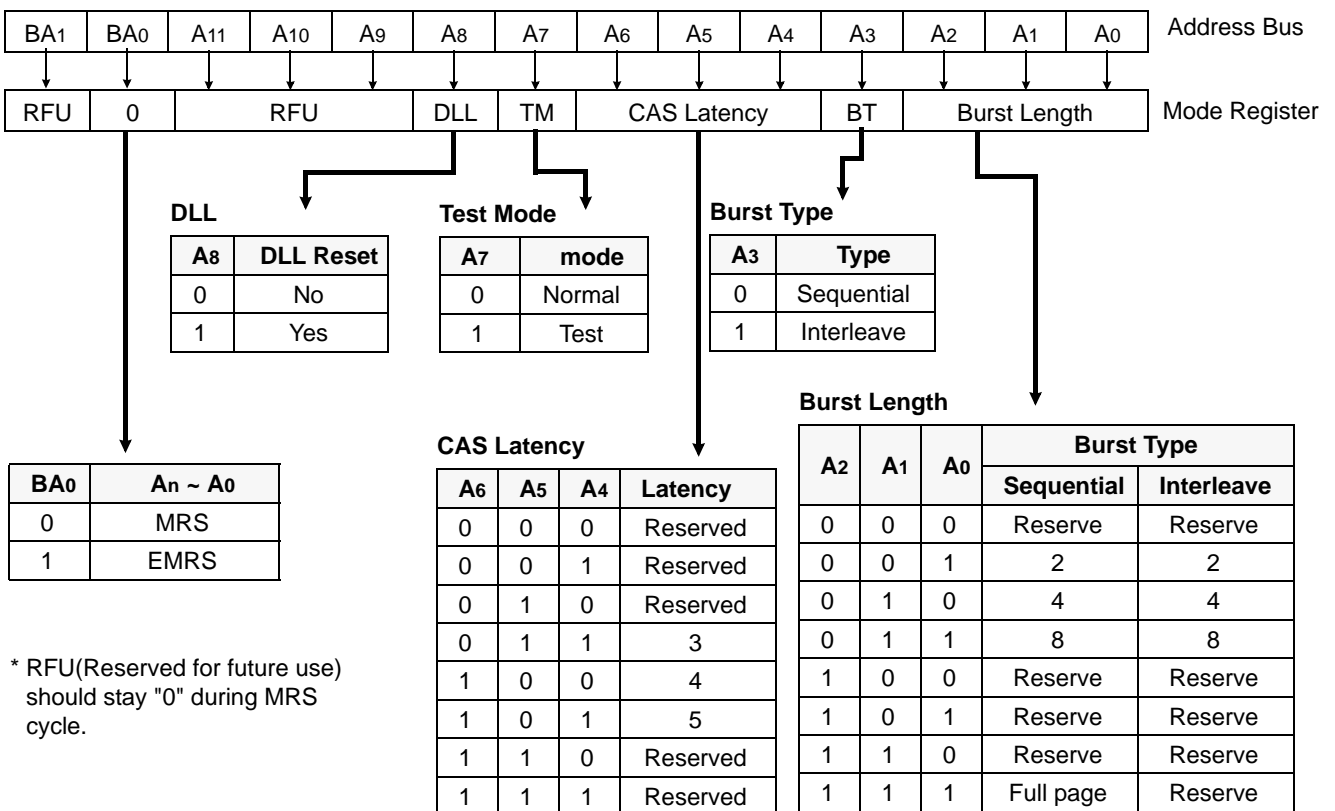
\*2 Sequence of 6&7 is regardless of the order.



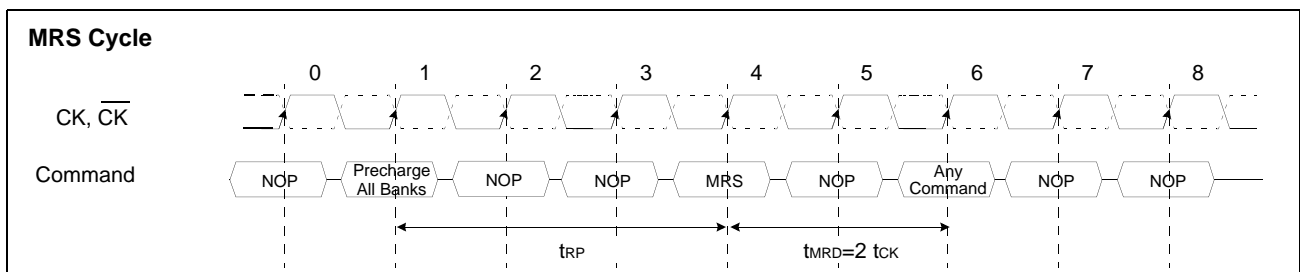
**\* When the operating frequency is changed, DLL reset should be required again.  
After DLL reset again, the minimum 200 cycles of clock input is needed to lock the DLL.**

**MODE REGISTER SET(MRS)**

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on CS, RAS, CAS and WE (The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A0 ~ A11 and BA0, BA1 in the same cycle as CS, RAS, CAS and WE going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, CAS latency(read latency from column address) uses A4 ~ A6. A7 is used for test mode. A8 is used for DLL reset. A7,A8, BA0 and BA1 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



\* RFU(Reserved for future use) should stay "0" during MRS cycle.

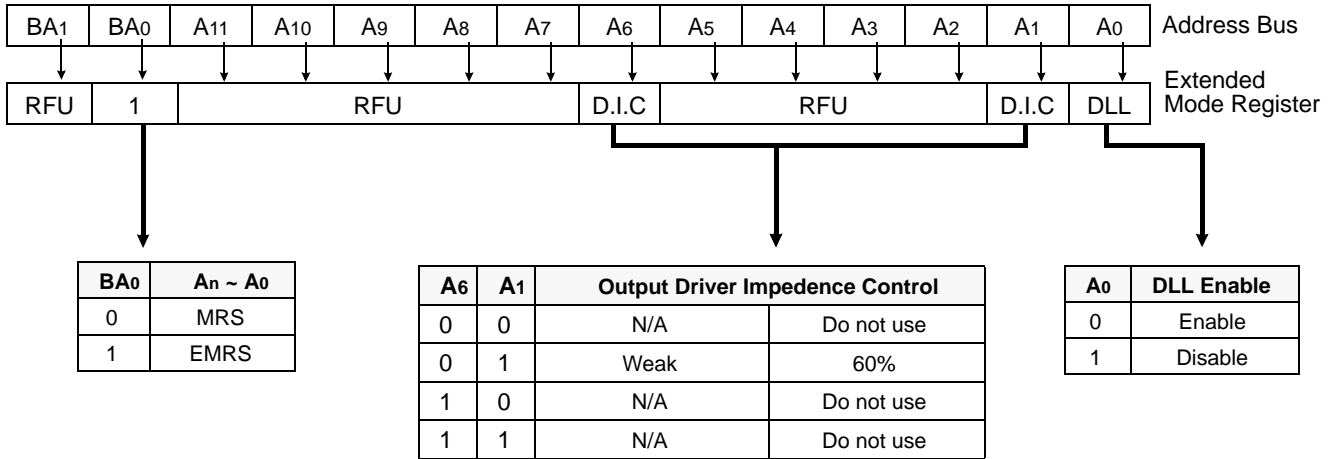


\*1 : MRS can be issued only at all banks precharge state.  
 \*2 : Minimum trp is required to issue MRS command.



**EXTENDED MODE REGISTER SET(EMRS)**

The extended mode register stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on CS, RAS, CAS, WE and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0, A2 ~ A5, A7 ~ A11 and BA1 in the same cycle as CS, RAS, CAS and WE going low are written in the extended mode register. A1 and A6 are used for setting driver strength to normal, weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0,A1,A6 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



\*1 : RFU(Reserved for future use) should stay "0" during EMRS cycle.

**Figure 7. Extended Mode Register set**

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 ~ 3.6	V
Voltage on VDD supply relative to Vss	VDD	-1.0 ~ 3.6	V
Voltage on VDD supply relative to Vss	VDDQ	-0.5 ~ 3.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>D</sub>	2.3	W
Short circuit current	I <sub>OS</sub>	50	mA

**Note** : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.  
 Functional operation should be restricted to recommended operating condition.  
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**POWER & DC OPERATING CONDITIONS(SSTL\_2 In/Out)**

Recommended operating conditions(Voltage referenced to Vss=0V, T<sub>A</sub>=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	VDD	2.375	2.50	2.625	V	1,7
Output Supply voltage	VDDQ	2.375	2.50	2.625	V	1,7
Reference voltage	VREF	0.49*VDDQ	-	0.51*VDDQ	V	2
Termination voltage	V <sub>tt</sub>	VREF-0.04	VREF	VREF+0.04	V	3
Input logic high voltage	V <sub>IH</sub> (DC)	VREF+0.15	-	VDDQ+0.30	V	4
Input logic low voltage	V <sub>IL</sub> (DC)	-0.30	-	VREF-0.15	V	5
Output logic high voltage	V <sub>OH</sub>	V <sub>tt</sub> +0.76	-	-	V	I <sub>OH</sub> =-15.2mA
Output logic low voltage	V <sub>OL</sub>	-	-	V <sub>tt</sub> -0.76	V	I <sub>OL</sub> =+15.2mA
Input leakage current	I <sub>IL</sub>	-5	-	5	uA	6
Output leakage current	I <sub>OL</sub>	-5	-	5	uA	6

- Note** :
- Under all conditions VDDQ must be less than or equal to VDD.
  - VREF is expected to equal 0.50\*VDDQ of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the VREF may not exceed + 2% of the DC value.
  - V<sub>tt</sub> of the transmitting device must track VREF of the receiving device.
  - V<sub>IH</sub>(max.)= VDDQ +1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
  - V<sub>IL</sub>(min.)= -1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
  - For any pin under test input of 0V ≤ V<sub>IN</sub> ≤ VDD is acceptable. For all other pins that are not under test V<sub>IN</sub>=0V.
  - For K4D263238A-GC33/36/40/45/50, VDD/VDDQ=2.5V ± 5%

**DC CHARACTERISTICS**

Recommended operating conditions Unless Otherwise Noted, TA=0 to 65°C)

Parameter	Symbol	Test Condition	Version					Unit	Note
			-33	-36	-40	-45	-50		
Operating Current (One Bank Active)	I <sub>CC1</sub>	Burst Length=2 t <sub>RC</sub> ≥ t <sub>RC</sub> (min) I <sub>OL</sub> =0mA, t <sub>CC</sub> = t <sub>CC</sub> (min)	430	410	380	370	350	mA	1
Precharge Standby Current in Power-down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = t <sub>CC</sub> (min)	75	70	65	65	65	mA	
Precharge Standby Current in Non Power-down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH</sub> (min), CS ≥ V <sub>IH</sub> (min), t <sub>CC</sub> = t <sub>CC</sub> (min)	120	115	110	100	100	mA	
Active Standby Current power-down mode	I <sub>CC3P</sub>	CKE ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = t <sub>CC</sub> (min)	120	110	100	100	100	mA	
Active Standby Current in in Non Power-down mode	I <sub>CC3N</sub>	CKE ≥ V <sub>IH</sub> (min), CS ≥ V <sub>IH</sub> (min), t <sub>CC</sub> = t <sub>CC</sub> (min)	310	280	240	230	230	mA	
Operating Current ( Burst Mode)	I <sub>CC4</sub>	I <sub>OL</sub> =0mA ,t <sub>CC</sub> = t <sub>CC</sub> (min), Page Burst, All Banks activated.	740	690	640	610	570	mA	
Refresh Current	I <sub>CC5</sub>	t <sub>RC</sub> ≥ t <sub>RFC</sub> (min)	300	290	280	270	260	mA	2
Self Refresh Current	I <sub>CC6</sub>	CKE ≤ 0.2V	4					mA	
Operating Current (4Bank interleaving)	I <sub>CC7</sub>	Burst Length=4 t <sub>RC</sub> ≥ t <sub>RC</sub> (min) I <sub>OL</sub> =0mA, t <sub>CC</sub> = t <sub>CC</sub> (min)	960	900	830	750	690	mA	

- Note** : 1. Measured with outputs open.  
2. Refresh period is 32ms.

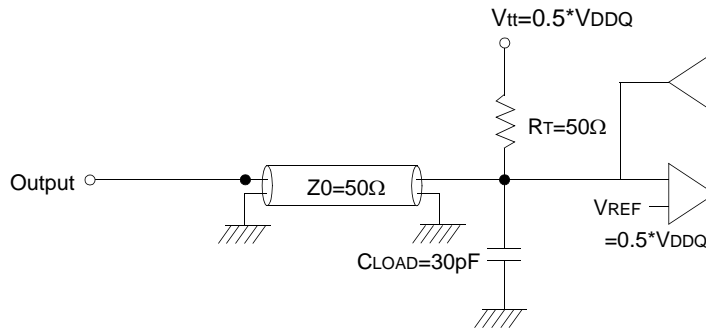
**AC INPUT OPERATING CONDITIONS**Recommended operating conditions(Voltage referenced to V<sub>SS</sub>=0V, V<sub>DD</sub>=2.5V±5%, V<sub>DDQ</sub>=2.5V±5%,TA=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input High (Logic 1) Voltage; DQ	V <sub>IH</sub>	V <sub>REF</sub> +0.35	-	-	V	
Input Low (Logic 0) Voltage; DQ	V <sub>IL</sub>	-	-	V <sub>REF</sub> -0.35	V	
Clock Input Differential Voltage; CK and $\overline{CK}$	V <sub>ID</sub>	0.7	-	V <sub>DDQ</sub> +0.6	V	1
Clock Input Crossing Point Voltage; CK and $\overline{CK}$	V <sub>IX</sub>	0.5*V <sub>DDQ</sub> -0.2	-	0.5*V <sub>DDQ</sub> +0.2	V	2

- Note** : 1. V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input level on  $\overline{CK}$   
2. The value of V<sub>IX</sub> is expected to equal 0.5\*V<sub>DDQ</sub> of the transmitting device and must track variations in the DC level of the same

**AC OPERATING TEST CONDITIONS** ( $V_{DD}=2.5V\pm 5\%$ ,  $T_A= 0$  to  $65^\circ C$ )

Parameter	Value	Unit	Note
Input reference voltage for CK(for single ended)	$0.50 \cdot V_{DDQ}$	V	
CK and $\overline{CK}$ signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input Levels( $V_{IH}/V_{IL}$ )	$V_{REF}+0.35/V_{REF}-0.35$	V	
Input timing measurement reference level	$V_{REF}$	V	
Output timing measurement reference level	$V_{tt}$	V	
Output load condition	See Fig.1		



(Fig. 1) Output Load Circuit

**CAPACITANCE** ( $V_{DD}=2.5V$ ,  $T_A= 25^\circ C$ ,  $f=1MHz$ )

Parameter	Symbol	Min	Max	Unit
Input capacitance(CK, $\overline{CK}$ )	$C_{IN1}$	1.0	5.0	pF
Input capacitance( $A_0\sim A_{11}$ , $BA_0\sim BA_1$ )	$C_{IN2}$	1.0	4.0	pF
Input capacitance (CKE, CS, RAS, CAS, WE)	$C_{IN3}$	1.0	4.0	pF
Data & DQS input/output capacitance(DQ0~DQ31)	$C_{OUT}$	1.0	6.5	pF
Input capacitance(DM0 ~ DM3)	$C_{IN4}$	1.0	6.5	pF

**DECOUPLING CAPACITANCE GUIDE LINE**

Recommended decoupling capacitance added to power line at board.

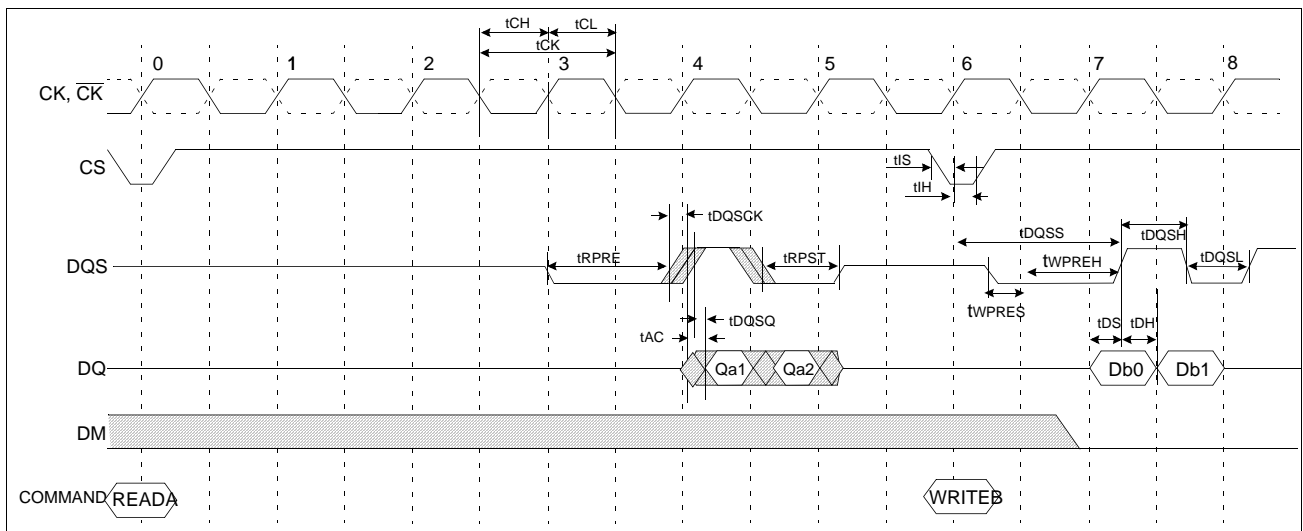
Parameter	Symbol	Value	Unit
Decoupling Capacitance between $V_{DD}$ and $V_{SS}$	$C_{DC1}$	$0.1 + 0.01$	$\mu F$
Decoupling Capacitance between $V_{DDQ}$ and $V_{SSQ}$	$C_{DC2}$	$0.1 + 0.01$	$\mu F$

- Note :**
- $V_{DD}$  and  $V_{DDQ}$  pins are separated each other.  
All  $V_{DD}$  pins are connected in chip. All  $V_{DDQ}$  pins are connected in chip.
  - $V_{SS}$  and  $V_{SSQ}$  pins are separated each other  
All  $V_{SS}$  pins are connected in chip. All  $V_{SSQ}$  pins are connected in chip.

AC CHARACTERISTICS

Parameter	Sym- bol	-33		-36		-40		-45		-50		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CK cycle time	t <sub>CK</sub>	CL=3	-	-	-	-	-	4.5	10	5.0	10	ns	
		CL=4	-	4	-	4	4.0	10	4.5	-	-	ns	
		CL=5	3.3	-	3.6	-	-	-	-	-	-	ns	
CK high level width	t <sub>CH</sub>	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>	
CK low level width	t <sub>CL</sub>	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>	
DQS out access time from CK	t <sub>DQSK</sub>	-0.6	0.6	-0.6	0.6	-0.6	0.6	-0.7	0.7	-0.7	0.7	ns	
Output access time from CK	t <sub>AC</sub>	-0.6	0.6	-0.6	0.6	-0.6	0.6	-0.7	0.7	-0.7	0.7	ns	
Data strobe edge to Dout edge	t <sub>DQSQ</sub>	-	0.35	-	0.40	-	0.4	-	0.45	-	0.45	ns	1
Read preamble	t <sub>RPRE</sub>	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t <sub>CK</sub>	
Read postamble	t <sub>RPST</sub>	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
CK to valid DQS-in	t <sub>DQSS</sub>	0.85	1.15	0.85	1.15	0.85	1.15	0.8	1.2	0.8	1.2	t <sub>CK</sub>	
DQS-In setup time	t <sub>WPRES</sub>	0	-	0	-	0	-	0	-	0	-	ns	
DQS-in hold time	t <sub>WPREH</sub>	0.35	-	0.35	-	0.35	-	0.3	-	0.3	-	t <sub>CK</sub>	
DQS write postamble	t <sub>WPST</sub>	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
DQS-In high level width	t <sub>DQSH</sub>	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
DQS-In low level width	t <sub>DQSL</sub>	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
Address and Control input setup	t <sub>IS</sub>	0.9	-	0.9	-	0.9	-	1.0	-	1.0	-	ns	
Address and Control input hold	t <sub>IH</sub>	0.9	-	0.9	-	0.9	-	1.0	-	1.0	-	ns	
DQ and DM setup time to DQS	t <sub>DS</sub>	0.35	-	0.40	-	0.4	-	0.45	-	0.45	-	ns	
DQ and DM hold time to DQS	t <sub>DH</sub>	0.35	-	0.40	-	0.4	-	0.45	-	0.45	-	ns	
Clock half period	t <sub>HP</sub>	t <sub>CLmin</sub> or t <sub>CHmin</sub>	-	t <sub>CLmin</sub> or t <sub>CHmin</sub>	-	t <sub>CLmin</sub> or t <sub>CHmin</sub>	-	t <sub>CLmin</sub> or t <sub>CHmin</sub>	-	t <sub>CLmin</sub> or t <sub>CHmin</sub>	-	ns	1
		t <sub>HP</sub>	-	t <sub>HP</sub>	-	t <sub>HP</sub>	-	t <sub>HP</sub>	-	t <sub>HP</sub>	-	ns	1
Data output hold time from DQS	t <sub>QH</sub>	t <sub>HP</sub> - 0.35	-	t <sub>HP</sub> - 0.4	-	t <sub>HP</sub> - 0.4	-	t <sub>HP</sub> - 0.45	-	t <sub>HP</sub> - 0.45	-	ns	1

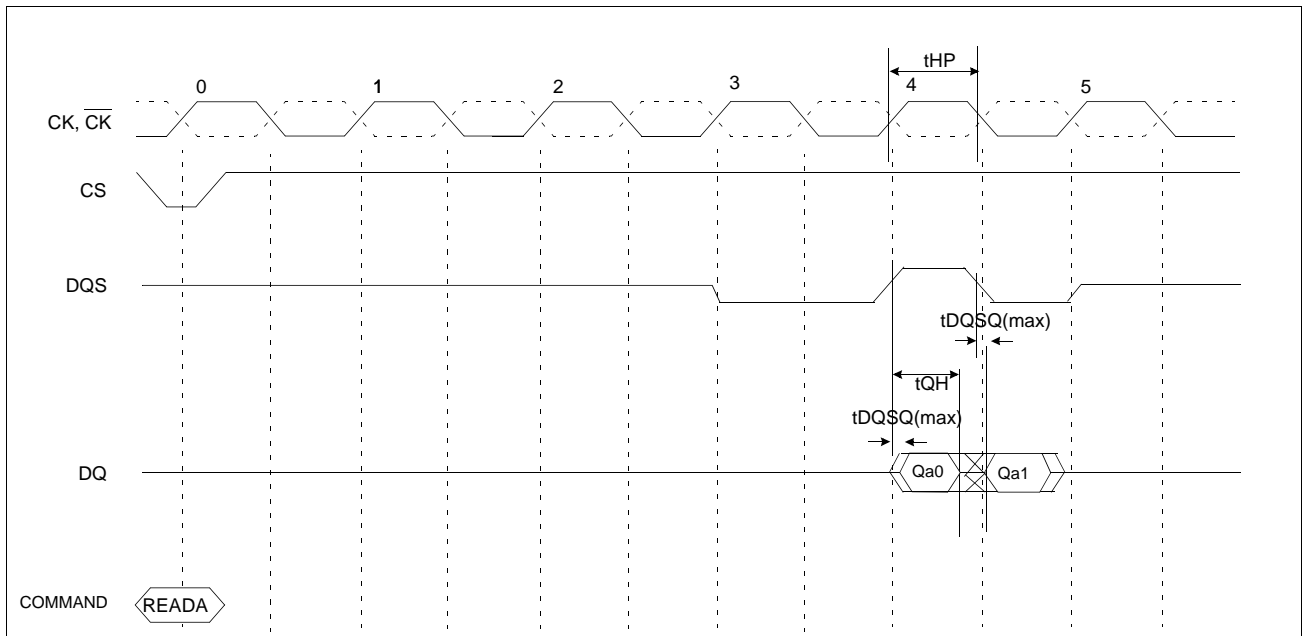
Simplified Timing @ BL=2, CL=4



Note 1 :

- The JEDEC DDR specification currently defines the output data valid window( $t_{DV}$ ) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of  $t_{DV}(=0.35t_{CK})$  artificially penalizes system timing budgets by assuming the worst case output valid window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term,  $t_{QH}$  which stands for data output hold time from DQS is defined to account for clock duty cycle variation and replaces  $t_{DV}$
- $t_{QHmin} = t_{HP}-X$  where
  - .  $t_{HP}$ =Minimum half clock period for any given cycle and is defined by clock high or clock low time( $t_{CH},t_{CL}$ )
  - .  $X$ =A frequency dependent timing allowance account for  $t_{DQSQmax}$

**$t_{QH}$  Timing (CL4, BL2)**



## AC CHARACTERISTICS (I)

Parameter	Symbol	-33		-36		-40		-45		-50		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Row cycle time	tRC	17	-	16	-	15	-	13	-	12	-	tCK	
Refresh row cycle time	tRFC	19	-	18	-	17	-	15	-	14	-	tCK	
Row active time	tRAS	12	100K	11	100K	10	100K	9	100K	8	100K	tCK	
RAS to CAS delay for Read	tRCDR	6	-	5	-	5	-	4	-	4	-	tCK	
RAS to CAS delay for Write	tRCDW	4	-	3	-	3	-	2	-	2	-	tCK	
Row precharge time	tRP	5	-	5	-	5	-	4	-	4	-	tCK	
Row active to Row active	tRRD	3	-	3	-	3	-	2	-	2	-	tCK	
Last data in to Row precharge @Normal Precharge	tWR	3	-	3	-	3	-	3	-	2	-	tCK	1
Last data in to Row precharge @Auto Precharge	tWR_A	3	-	3	-	3	-	3	-	3	-	tCK	1
Last data in to Read command	tCDLR	2	-	2	-	2	-	2	-	2	-	tCK	1
Col. address to Col. address	tCCD	1	-	1	-	1	-	1	-	1	-	tCK	
Mode register set cycle time	tMRD	2	-	2	-	2	-	2	-	2	-	tCK	
Auto precharge write recovery + Precharge	tDAL	8	-	8	-	8	-	7	-	7	-	tCK	
Exit self refresh to read com-	tXSR	200	-	200	-	200	-	200	-	200	-	tCK	
Power down exit time	tPDEX	1tCK+tIS	-	1tCK+tIS	-	1tCK+tIS	-	1tCK+tIS	-	1tCK+tIS	-	ns	
Refresh interval time	tREF	7.8	-	7.8	-	7.8	-	7.8	-	7.8	-	us	

Note : 1. For normal write operation, even numbers of Din are to be written inside DRAM

(Unit : Number of Clock)

## AC CHARACTERISTICS (II)

## K4D263238A-GC33

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
300MHz ( 3.3ns )	5	17	19	12	6	4	5	3	8	tCK
275MHz ( 3.6ns )	5	16	18	11	5	3	5	3	8	tCK
250MHz ( 4.0ns )	4	15	17	10	5	3	5	3	8	tCK
222MHz ( 4.5ns )	4	13	15	9	4	2	4	2	7	tCK
200MHz ( 5.0ns )	3	12	14	8	4	2	4	2	7	tCK

## K4D263238A-GC36

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
275MHz ( 3.6ns )	5	16	18	11	5	3	5	3	8	tCK
250MHz ( 4.0ns )	4	15	17	10	5	3	5	3	8	tCK
222MHz ( 4.5ns )	4	13	15	9	4	2	4	2	7	tCK
200MHz ( 5.0ns )	3	12	14	8	4	2	4	2	7	tCK

**K4D263238A-GC40**

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
250MHz ( 4.0ns )	4	15	17	10	5	3	5	3	8	tCK
222MHz ( 4.5ns )	4	13	15	9	4	2	4	2	7	tCK
200MHz ( 5.0ns )	3	12	14	8	4	2	4	2	7	tCK

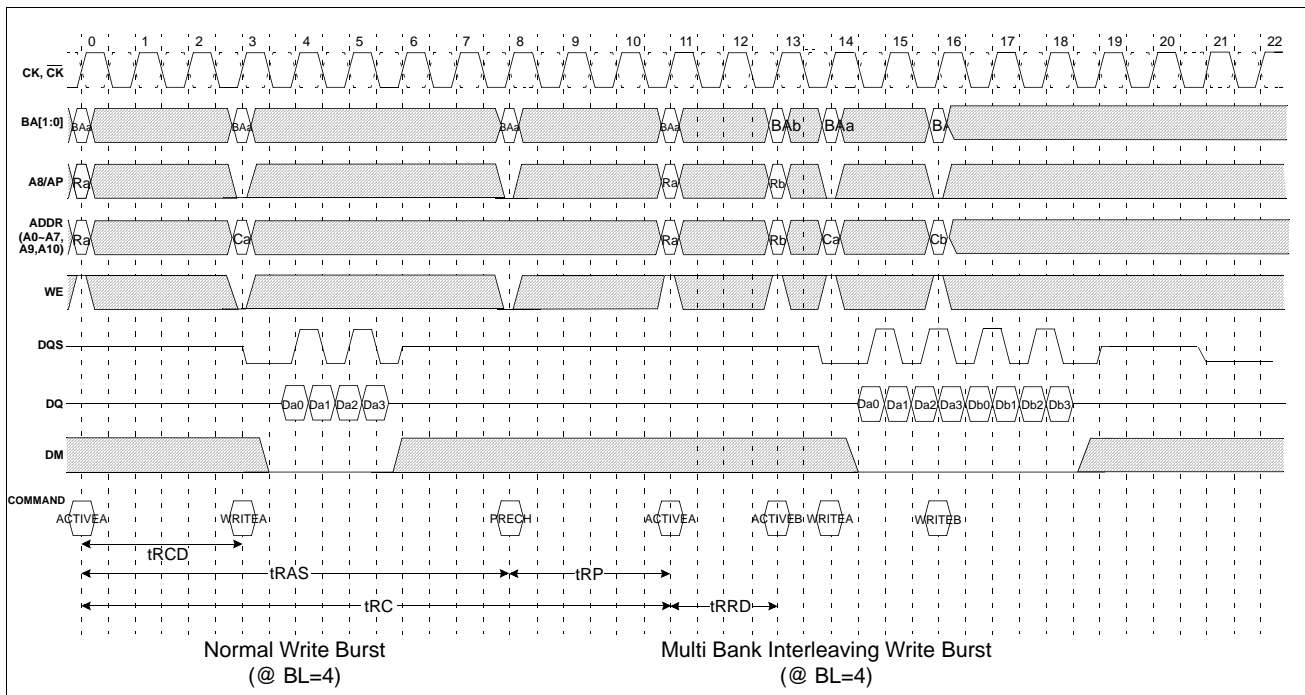
**K4D263238A-GC45**

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
222MHz ( 4.5ns )	4/3	13	15	9	4	2	4	2	7	tCK
200MHz ( 5.0ns )	3	12	14	8	4	2	4	2	7	tCK

**K4D263238A-GC50**

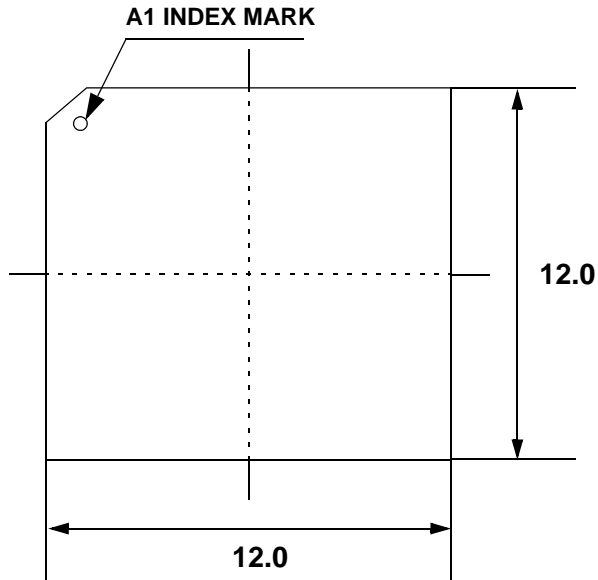
Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
200MHz ( 5.0ns )	3	12	14	8	4	2	4	2	7	tCK

**Simplified Timing(2) @ BL=4**

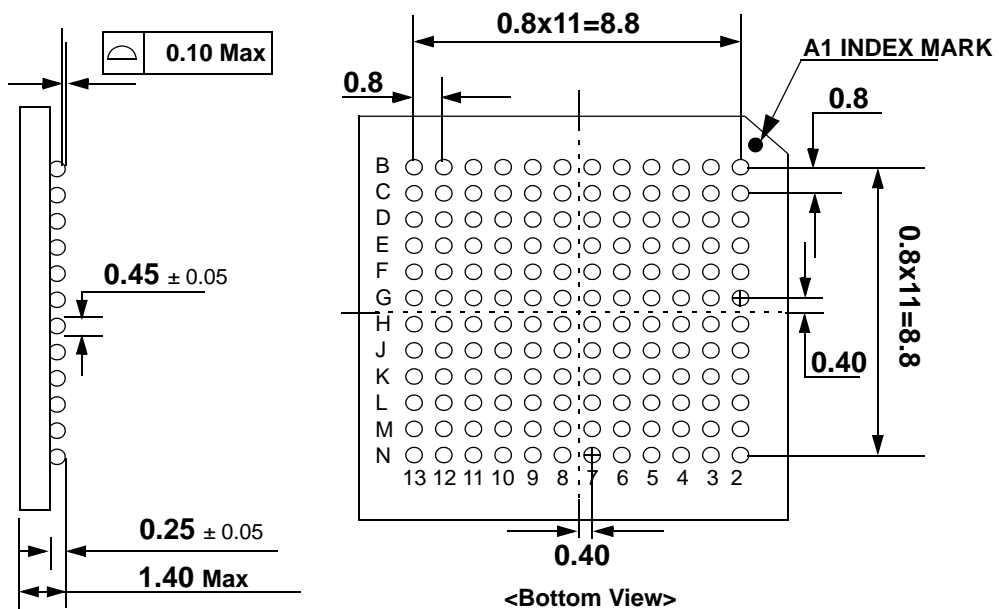




PACKAGE DIMENSIONS (144-Ball FBGA)



<Top View>



<Bottom View>

Unit : mm