



F100141 8-Bit Shift Register

General Description

The F100141 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

The circuit operating mode is determined by the Select inputs S_0 and S_1 , which are internally decoded to select either

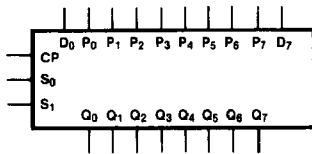
"parallel entry", "hold", "shift left" or "shift right" as described in the Truth Table. All inputs have 50 k Ω pull-down resistors.

Refer to the F100341 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

Logic Symbol

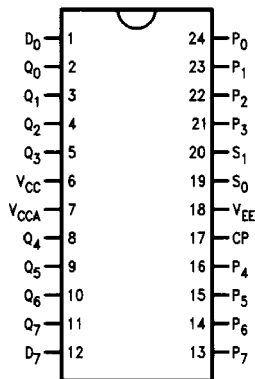


TL/F/9856-1

Pin Names	Description
CP	Clock Input
S_0, S_1	Select Inputs
D_0, D_7	Serial Inputs
P_0-P_7	Parallel Inputs
Q_0-Q_7	Data Outputs

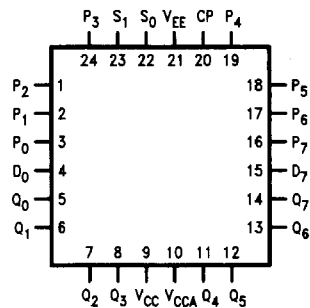
Connection Diagrams

24-Pin DIP



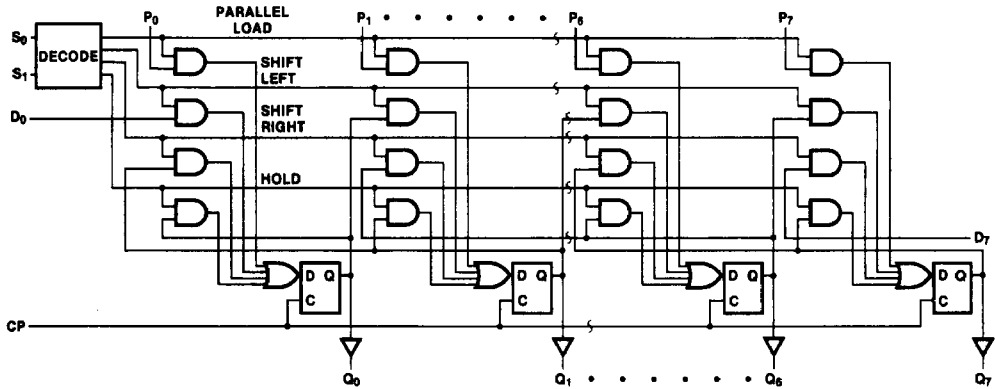
TL/F/9856-2

24-Pin Quad Cerpak



TL/F/9856-3

Logic Diagram



TL/F/9856-5

Truth Table

Function	Inputs					Outputs							
	D ₇	D ₀	S ₁	S ₀	CP	Q ₇	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀
Load Register	X	X	L	L	↗	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀
Shift Left	X	L	L	H	↗	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀	L
Shift Left	X	H	L	H	↗	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀	H
Shift Right	L	X	H	L	↗	L	Q ₇	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁
Shift Right	H	X	H	L	↗	H	Q ₇	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H								
Hold	X	X	X	X	L								

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 ↗ = LOW-to-HIGH transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to +150°C
Maximum Junction Temperature (T_J) +150°C

Case Temperature under Bias (T_C) 0°C to +85°C
V_{EE} Pin Potential to Ground Pin -7.0V to +0.5V
Input Voltage (DC) V_{EE} to +0.5V
Output Current (DC Output HIGH) -50 mA
Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	-1025	-955	-880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1810	-1705	-1620			
V _{OHC}	Output HIGH Voltage	-1035			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1610			
V _{IH}	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	-1020		-870	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1810		-1605			
V _{OHC}	Output HIGH Voltage	-1030			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1595			
V _{IH}	Input HIGH Voltage	-1150		-870	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	-1035		-880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1830		-1620			
V _{OHC}	Output HIGH Voltage	-1045			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1610			
V _{IH}	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	-1830		-1490	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current D_n, P_n, S_n CP			220 550	μA	$V_{IN} = V_{IH}(\text{Max})$
I_{EE}	Power Supply Current	-238	-170	-119	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	275		275		255		MHz	Figures 2 and 3
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	2.40	1.10	2.30	1.10	2.50	ns	Figures 1 and 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	
t_S	Setup Time D_n, P_n S_n	0.85 2.20		0.85 2.20		0.85 2.20		ns	Figure 4
t_H	Hold D_n, P_n S_n	0.60 0.10		0.60 0.10		0.60 0.10		ns	
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figure 3

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	300		300		280		MHz	Figures 2 and 3
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	2.20	1.10	2.10	1.10	2.30	ns	Figures 1 and 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.40	ns	
t_S	Setup Time D_n, P_n S_n	0.75 2.10		0.75 2.10		0.75 2.10		ns	Figure 4
t_H	Hold D_n, P_n S_n	0.50 0		0.50 0		0.50 0		ns	
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figure 3

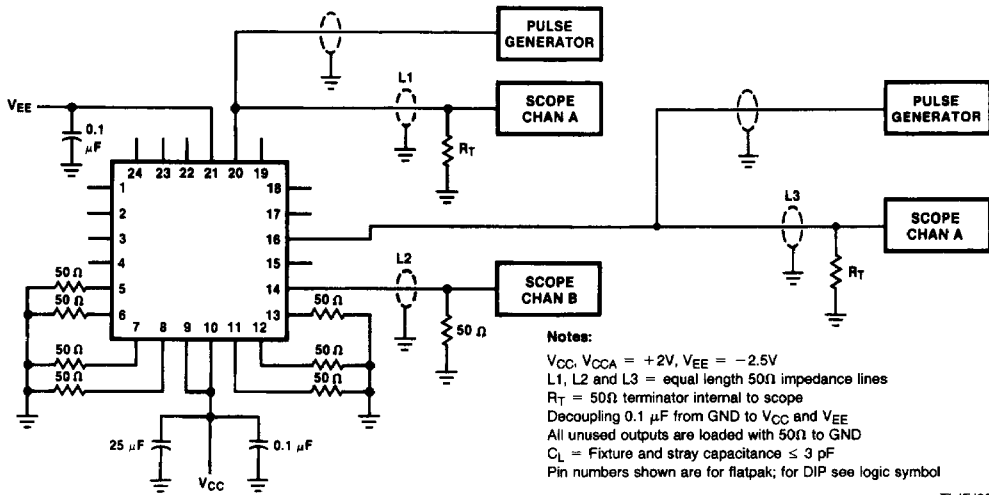
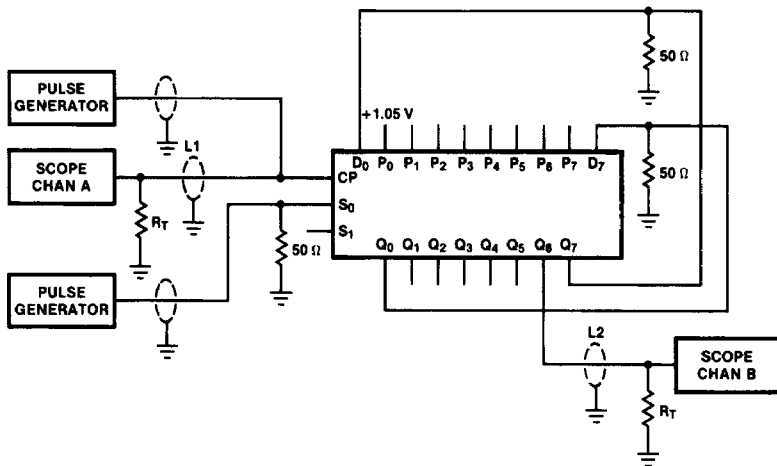


FIGURE 1. AC Test Circuit

TL/F/9856-6



Notes:

- For shift right mode pulse generator connected to S_0 is moved to S_1 .
- Pulse generator connected to S_1 has a LOW frequency 99% duty cycle, which allows occasional parallel load.
- The feedback path from output to input should be as short as possible.

FIGURE 2. Shift Frequency Test Circuit (Shift Left)

TL/F/9856-7

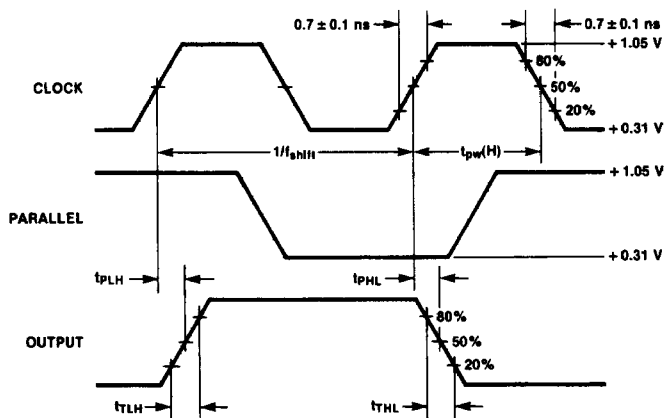
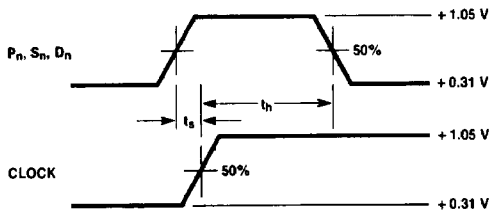


FIGURE 3. Propagation Delay and Transition Times

TL/F/9856-8



Note:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

TL/F/9856-9

FIGURE 4. Setup and Hold Times