



LP62S4096E-T Series

512K X 8 BIT LOW VOLTAGE CMOS SRAM

Document Title

512K X 8 BIT LOW VOLTAGE CMOS SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
2.0	Change Vccmax from 3.3V to 3.6V Add product family and 55ns specification	January 25, 2002	



LP62S4096E-T Series

512K X 8 BIT LOW VOLTAGE CMOS SRAM

Features

- Power supply range: 2.7V to 3.6V
- Access times: 55ns / 70ns (max.)
- Current:
 - Very low power version: Operating: 30mA (max.)
 - Standby: 10µA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2V (min.)
- Available in 32-pin TSOP/TSSOP 36-ball CSP package

General Description

The LP62S4096E-T is a low operating current 4,194,304-bit static random access memory organized as 524,288 words by 8 bits and operates on a low power supply range: 2.7V to 3.3V. It is built using AMIC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Two chip enable inputs are provided for POWER-DOWN and device enable and an output enable input is included for easy interfacing.

Data retention is guaranteed at a power supply voltage as low as 2V.

- CE2 pin for CSP package only

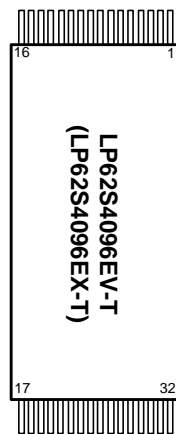
Product Family

Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I _{CCDR} , Typ.)	Standby (I _{SB1} , Typ.)	Operating (I _{CC2} , Typ.)	
LP62S4096E-T	-25°C ~ +85°C	2.7V~3.6V	55ns / 70ns	0.08µA	0.3µA	5mA	32L TSOP 32L TSSOP 36B CSP

1. Typical values are measured at VCC = 3.0V, T_A = 25°C and not 100% tested.
2. Data retention current VCC = 2.0V.

Pin Configurations

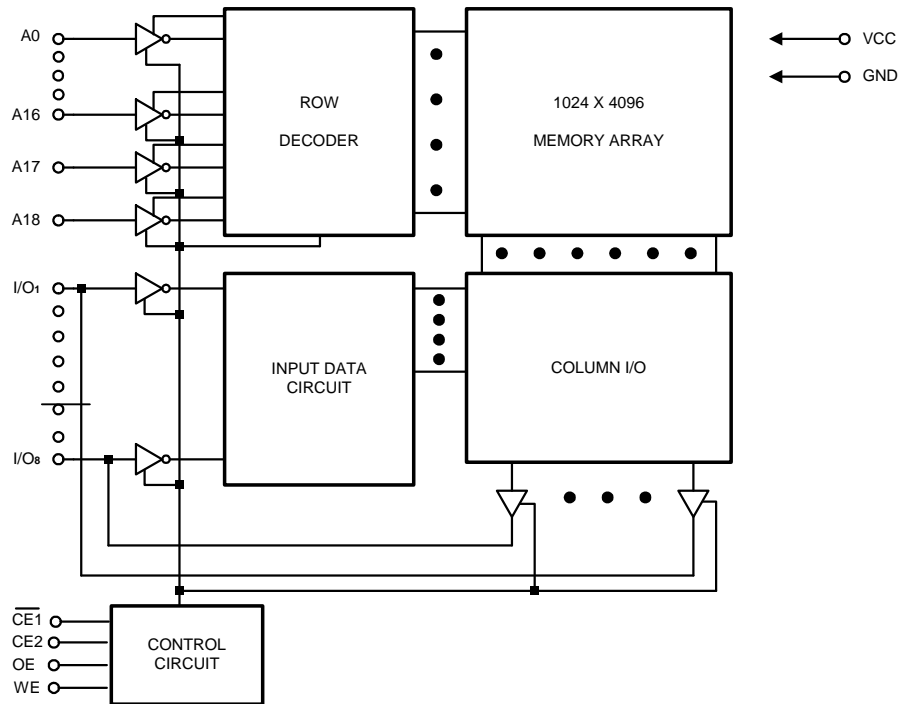
■ TSOP/(TSSOP)



Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A11	A9	A8	A13	\overline{WE}	A17	A15	VCC	A18	A16	A14	A12	A7	A6	A5	A4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A3	A2	A1	A0	I/O ₁	I/O ₂	I/O ₃	GND	I/O ₄	I/O ₅	I/O ₆	I/O ₇	I/O ₈	$\overline{CE1}$	A10	\overline{OE}

■ CSP (Chip Size Package) 36-pin Top View

	1	2	3	4	5	6
A	A0	A1	CE2	A3	A6	A8
B	I/O ₅	A2	\overline{WE}	A4	A7	I/O ₁
C	I/O ₆		NC	A5		I/O ₂
D	GND					VCC
E	VCC					GND
F	I/O ₇		A18	A17		I/O ₃
G	I/O ₈	\overline{OE}	$\overline{CE1}$	A16	A15	I/O ₄
H	A9	A10	A11	A12	A13	A14

Block Diagram

Pin Description

Symbol	Description
A0 - A18	Address Inputs
I/O ₁ - I/O ₈	Data Input/Outputs
GND	Ground
$\overline{CE1}$, $\overline{CE2}$	Chip Enable
\overline{OE}	Output Enable
\overline{WE}	Write Enable
VCC	Power Supply

Recommended DC Operating Conditions

 (T_A = -25°C to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3.0	3.6	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V _{IL}	Input Low Voltage	-0.3	0	+0.6	V
C _L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-



Absolute Maximum Ratings*

VCC to GND ----- -0.5V to + 4.0V
 IN, IN/OUT Volt to GND----- -0.5V to VCC + 0.5V
 Operating Temperature, Topr ----- -25°C to + 85°C
 Storage Temperature, Tstg ----- -55°C to + 125°C
 Temperature Under Bias, Tbias ----- -10°C to + 85°C
 Power Dissipation, P_T ----- 0.7W

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = -25°C to + 85°C, VCC = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	LP62S4096E-55LLT / 70LLT			Unit	Conditions
		Min.	Typ.	Max.		
I _{LI}	Input Leakage Current	-	-	1	μA	V _{IN} = GND to VCC
I _{LO}	Output Leakage Current	-	-	1	μA	$\overline{CE1} = V_{IH}$, CE2= V _{IL} or $\overline{OE} = V_{IH}$ $\overline{WE} = V_{IL}$ V _{I/O} = GND to VCC
I _{CC}	Active Power Supply Current	-	-	5	mA	$\overline{CE1} = V_{IL}$, CE2= V _{IH} I _{I/O} = 0mA
I _{CC1}	Dynamic Operating Current	-	20	30	mA	Min. Cycle, Duty = 100%, $\overline{CE1} = V_{IL}$ CE2= V _{IH} , I _{I/O} = 0mA
I _{CC2}	Dynamic Operating Current	-	5	15	mA	$\overline{CE1} = V_{IL}$, CE2= V _{IH} , V _{IH} = VCC V _{IL} = 0V, f = 1MHz I _{I/O} = 0mA
I _{SB}	Standby Power	-	-	1	mA	VCC ≤ 3.3V $\overline{CE1} = V_{IH}$, CE2= V _{IL}
I _{SB1}	Supply Current	-	0.3	10	μA	VCC ≤ 3.3V $\overline{CE1} \geq VCC - 0.2V$, or CE2 ≤ 0.2V V _{IN} ≤ 0.2V
V _{OL}	Output Low Voltage	-	-	0.4	V	I _{OL} = 2.1mA
V _{OH}	Output High Voltage	2.2	-	-	V	I _{OH} = -1.0mA

Truth Table

Mode	$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB} , I_{SB1}
Standby	X	L	X	X	High Z	I_{SB} , I_{SB1}
Output Disable	L	H	H	H	High Z	I_{CC} , I_{CC1} , I_{CC2}
Read	L	H	L	H	Dout	I_{CC} , I_{CC1} , I_{CC2}
Write	L	H	X	L	Din	I_{CC} , I_{CC1} , I_{CC2}

Note: X = H or L

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}^*	Input Capacitance		6	pF	$V_{IN} = 0V$
C_{IO}^*	Input/Output Capacitance		8	pF	$V_{IO} = 0V$

* These parameters are sampled and not 100% tested.

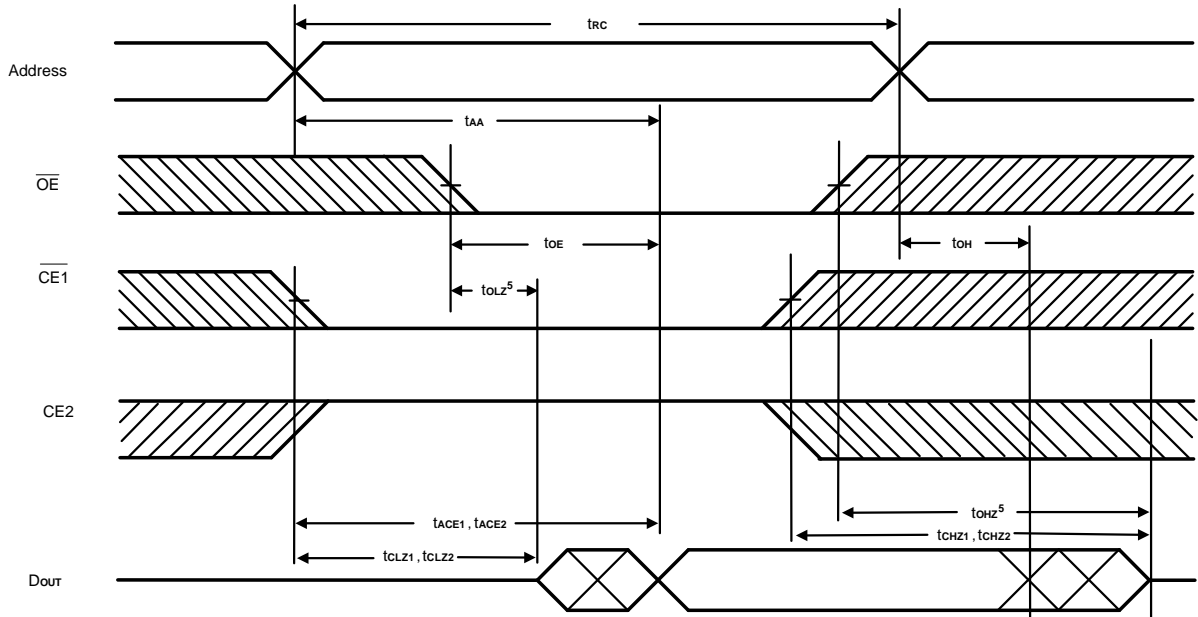
AC Characteristics ($T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7V$ to $3.6V$)

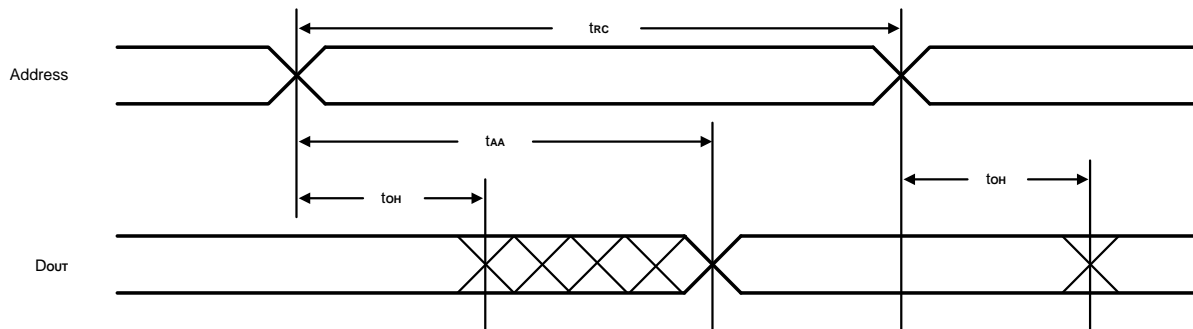
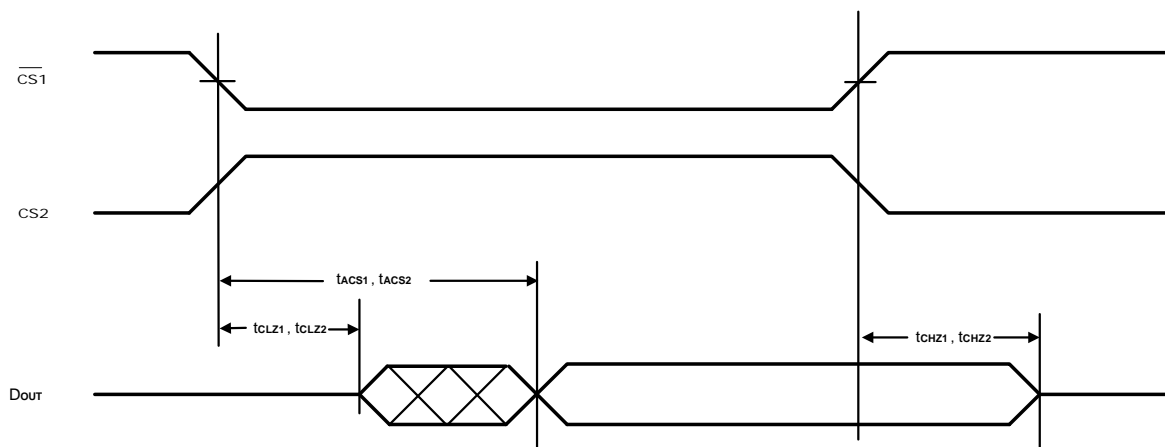
Symbol	Parameter	LP62S4096E-55LLT		LP62S4096E-70LLT		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55	-	70	-	ns
t_{AA}	Address Access Time	-	55	-	70	ns
t_{ACE1} , t_{ACE2}	Chip Enable Access Time	-	55	-	70	ns
t_{OE}	Output Enable to Output Valid	-	30		35	ns
t_{CLZ1} , t_{CLZ2}	Chip Enable to Output in Low Z	10	-	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	ns
t_{CHZ1} , t_{CHZ2}	Chip Disable to Output in High Z	0	20	0	25	ns
t_{OHZ}	Output Disable to Output in High Z	0	20	0	25	ns
t_{OH}	Output Hold from Address Change	5	-	5	-	ns

AC Characteristics (continued)

Symbol	Parameter	LP62S4096E-55LLT		LP62S4096E-70LLT		Unit
		Min.	Max.	Min.	Max.	
Write Cycle						
t _{wc}	Write Cycle Time	55	-	70	-	ns
t _{cw1}	Chip Enable to End of Write	50	-	60	-	ns
t _{as}	Address Setup Time	0	-	0	-	ns
t _{aw}	Address Valid to End of Write	50	-	60	-	ns
t _{wp}	Write Pulse Width	40	-	50	-	ns
t _{wr}	Write Recovery Time	0	-	0	-	ns
t _{whz}	Write to Output in High Z	0	25	0	25	ns
t _{dw}	Data to Write Time Overlap	25	-	30	-	ns
t _{dh}	Data Hold from Write Time	0	-	0	-	ns
t _{ow}	Output Active from End of Write	5	-	5	-	ns

Notes: t_{chz}, t_{ohz} and t_{whz} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms Read Cycle 1⁽¹⁾


Timing Waveforms (continued)
Read Cycle 2 (1, 2, 4)

Read Cycle 3 (1, 3, 4)


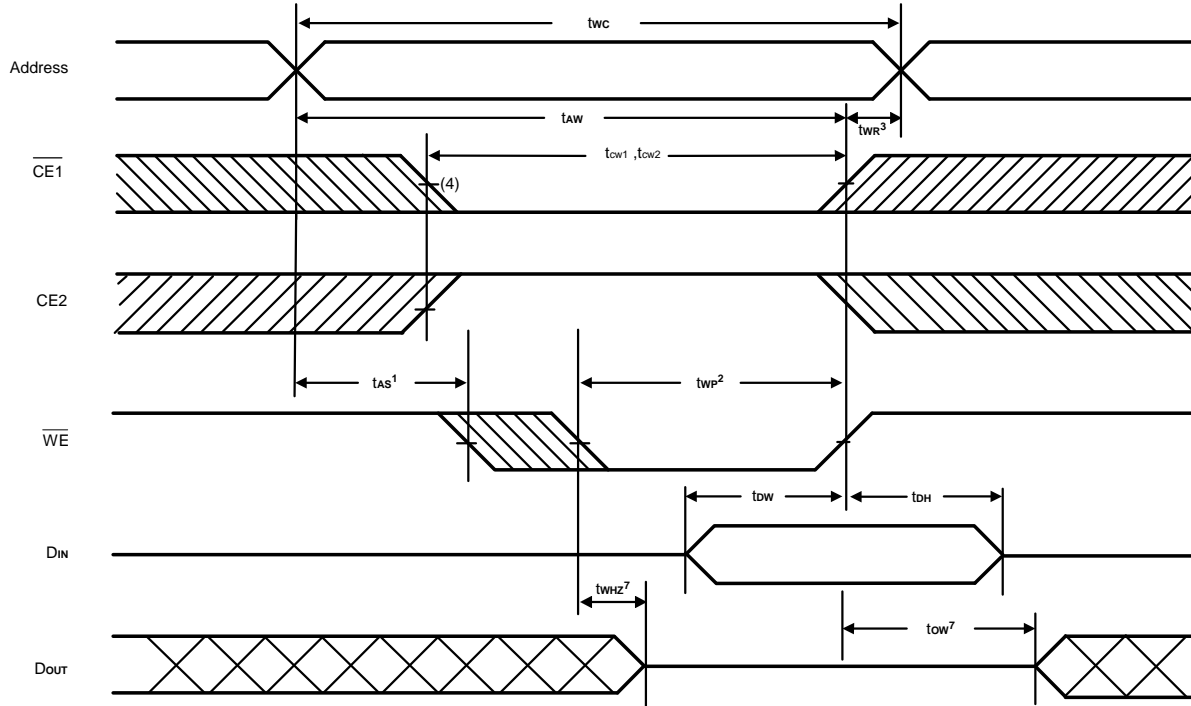
Notes: 1. \overline{WE} is high for Read Cycle.

2. Device is continuously enabled, $\overline{CE1} = V_{IL}$ or $CE2 = V_{IH}$.

3. Address valid prior to or coincident with $\overline{CE1}$ transition low or $CE2$ transition high.

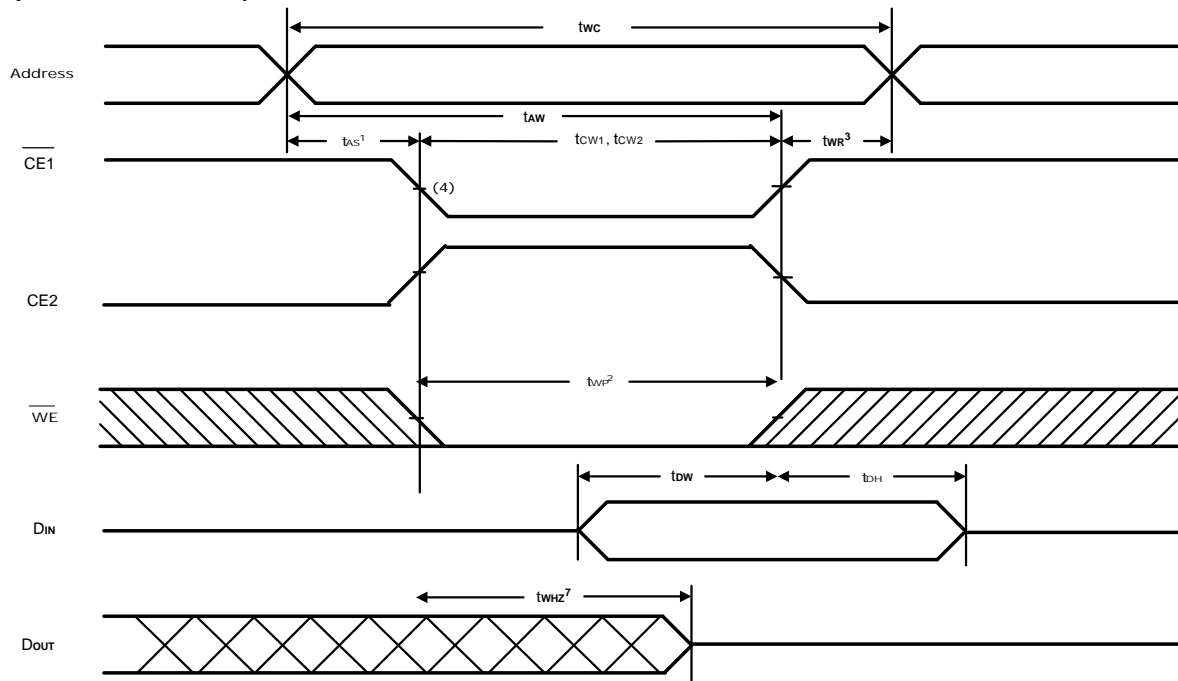
4. $\overline{OE} = V_{IL}$.

5. Transition is measured $\pm 500mV$ from steady state. This parameter is sampled and not 100% tested.

Timing Waveforms (continued)
Write Cycle 1⁽⁶⁾
(Write Enable Controlled)




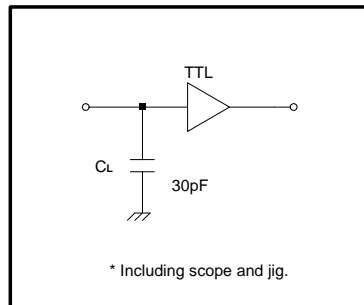
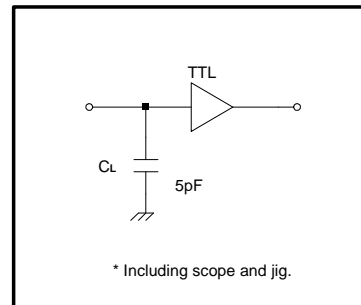
Write Cycle 2⁽⁶⁾
(Chip Enable Controlled)



- Notes:
1. t_{as} is measured from the address valid to the beginning of Write.
 2. A Write occurs during the overlap (t_{wr}) of a low $\overline{CE1}$ or high CE2 , and a low \overline{WE} .
 3. t_{wr} is measured from the earliest of $\overline{CE1}$ or \overline{WE} going high or CE2 going low \overline{WE} going high to the end of the Write cycle.
 4. If the $\overline{CE1}$ low or CE2 high transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, outputs remain in a high impedance state.
 5. t_{cw} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of Write.
 6. \overline{OE} level is high or low.
 7. Transition is measured $\pm 500mV$ from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

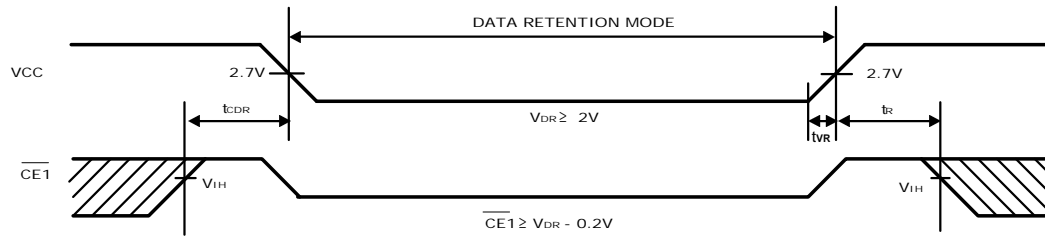
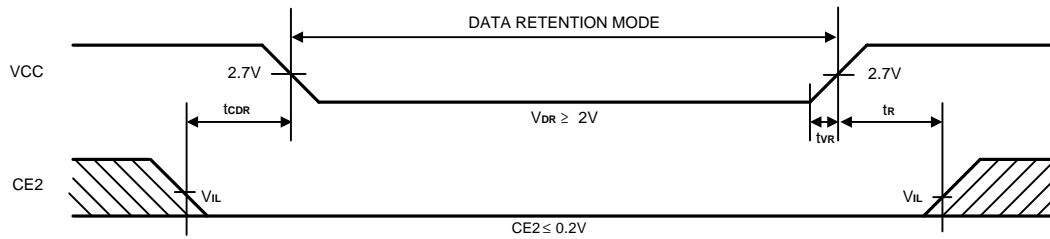
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2


Figure 1. Output Load

Figure 2. Output Load for t_{CLZ} , t_{OHZ} , t_{OL} , t_{CHZ} , t_{WHZ} , and t_{ow}
Data Retention Characteristics ($T_A = -25^\circ\text{C}$ to 85°C)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention		2.0	-	3.6	V	$\overline{CE1} \geq VCC - 0.2V$, or $CE2 \leq 0.2V$
I_{CCDR}	Data Retention Current	LL-Version	-	0.08	3*	μA	$VCC = 2.0V$, $\overline{CE1} \geq VCC - 0.2V$, or $CE2 \leq 0.2V$ $V_{IN} \leq 0V$
t_{CDR}	Chip Disable to Data Retention Time		0	-	-	ns	See Retention Waveform
t_r	Operation Recovery Time		t_{RC}	-	-	ns	
t_{VR}	VCC Rising Time from Data Retention Voltage to Operating Voltage		5	-	-	ms	

* LP62S4096E-55LLT / 70LLT

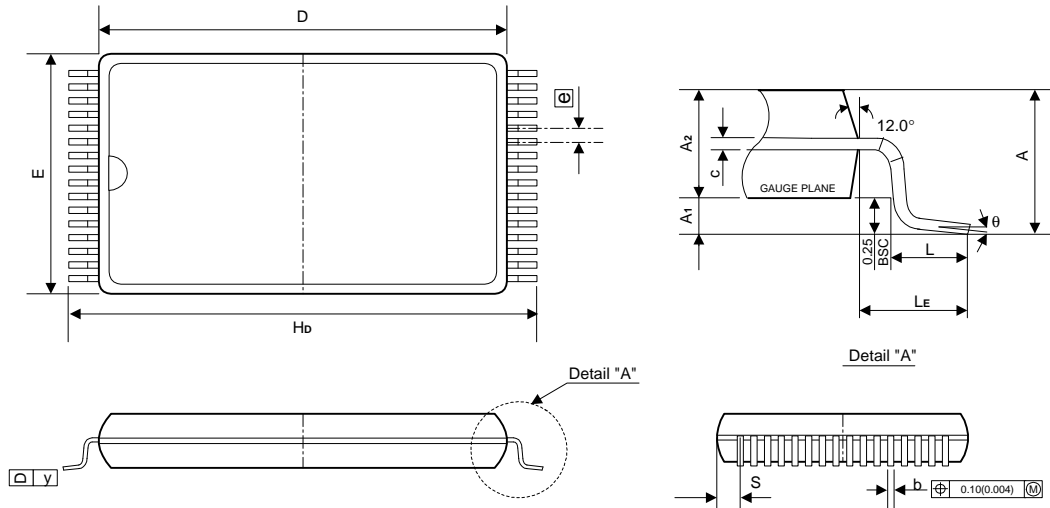
I_{CCDR} : max. $1\mu\text{A}$ at $T_A = 0^\circ\text{C}$ to $+40^\circ\text{C}$

Low VCC Data Retention Waveform (1) ($\overline{CE1}$ Controlled)

Low VCC Data Retention Waveform (2) ($CE2$ Controlled)

Ordering Information

Part No.	Access Time(ns)	Operating Current Max.(mA)	Standby Current Max.(uA)	Package
LP62S4096EV-55LLT	55	30	10	32L TSOP
LP62S4096EX-55LLT	55	30	10	32L TSSOP
LP62S4096EU-55LLT	55	30	10	36L CSP
LP62S4096EV-70LLT	70	30	10	32L TSOP
LP62S4096EX-70LLT	70	30	10	32L TSSOP
LP62S4096EU-70LLT	70	30	10	36L CSP

Package Information
TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm



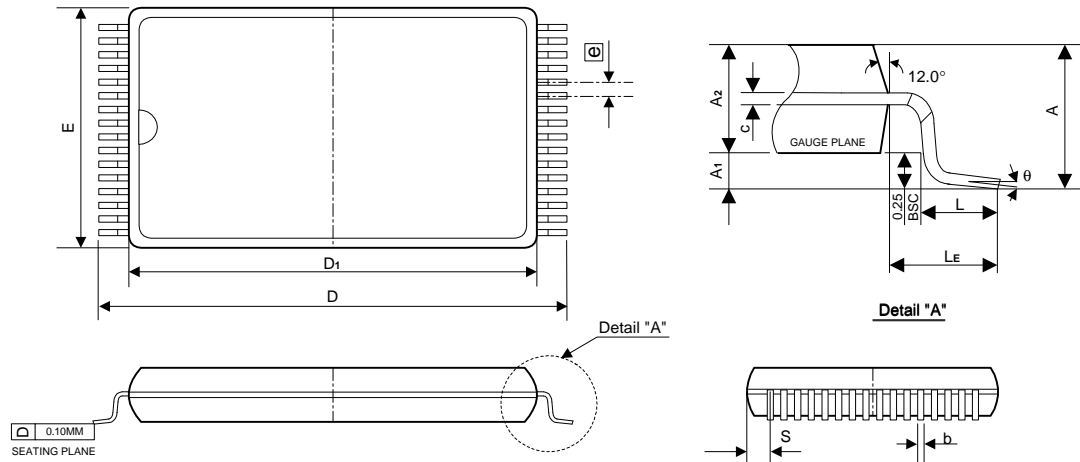
Symbol	Dimensions in inches	Dimensions in mm
A	0.047 Max.	1.20 Max.
A ₁	0.004±0.002	0.10±0.05
A ₂	0.039±0.002	1.00±0.05
b	0.008±0.001	0.20±0.03
c	0.006±0.001	0.15±0.02
D	0.724±0.004	18.40±0.10
E	0.315±0.004	8.00±0.10
e ₁	0.020 TYP.	0.50 TYP.
H _b	0.787±0.007	20.00±0.20
L	0.020±0.004	0.50±0.10
LE	0.031 TYP.	0.80 TYP.
S	0.0167 TYP.	0.425 TYP.
Y	0.004 Max.	0.10 Max.
θ	0° ~ 6°	0° ~ 6°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e₁ is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information
TSSOP 32L TYPE I (8 X 13.4mm) Outline Dimensions

unit: inches/mm



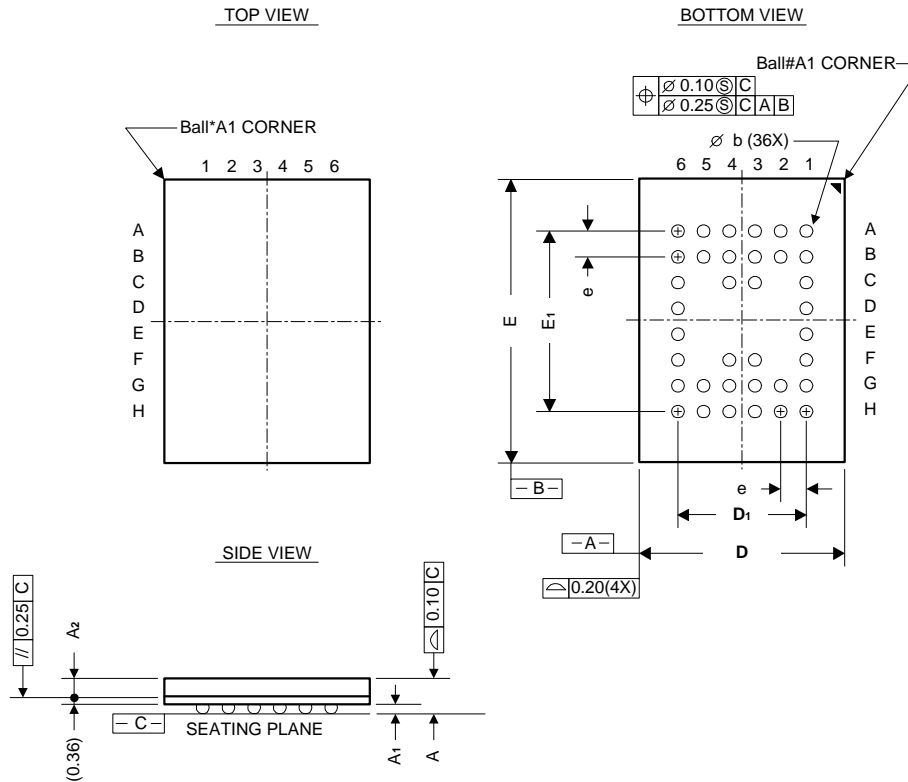
Symbol	Dimensions in inches	Dimensions in mm
A	0.049 Max.	1.25 Max.
A1	0.002 Min.	0.05 Min.
A2	0.039±0.002	1.00±0.05
b	0.008±0.001	0.20±0.03
c	0.006±0.0003	0.15±0.008
E	0.315±0.004	8.00±0.10
e	0.020 TYP.	0.50 TYP.
D	0.528±0.008	13.40±0.20
D1	0.465±0.004	11.80±0.10
L	0.02±0.008	0.50±0.20
LE	0.0266 Min.	0.675 Min.
S	0.0109 TYP.	0.278 TYP.
y	0.004 Max.	0.10 Max.
θ	0° ~ 6°	0° ~ 6°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e₁ is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information
36LD CSP (6 x 8 mm) Outline Dimensions

unit: mm



Symbol	Dimensions in mm		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A ₁	0.16	0.21	0.26
A ₂	0.48	0.53	0.58
D	5.80	6.00	6.20
D ₁	---	3.75	---
E ₁	---	5.25	---
e	---	0.75	---
b	0.25	0.30	0.35

Note:

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.
THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. BALL PAD OPENING OF SUBSTRATE IS Φ 0.25mm (SMD)
SUGGEST TO DESIGN THE PCB LAND SIZE AS Φ 0.25mm (NSMD)