



## 256MB – 32Mx64 DDR2 SDRAM UNBUFFERED

### FEATURES

- 240-pin, dual in-line memory module
- Fast data transfer rates: PC2-6400\*, PC2-5300\*, PC2-4200 and PC2-3200
- Utilizes 800\*, 667\*, 533 and 400 MT/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- JEDEC standard 1.8V I/O (SSTL\_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Gold edge contacts
- Single Rank
- RoHS compliant
- Package option
  - 240 Pin DIMM
  - PCB – 30.00mm (1.181") TYP

### DESCRIPTION

The WV3HG32M64EEU is a 32Mx64 Double Data Rate DDR2 SDRAM high density module. This memory module consists of eight 32Mx8 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 240-pin DIMM FR4 substrate.

\* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

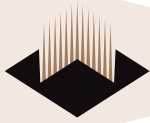
NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

### OPERATING FREQUENCIES

	PC2-3200	PC2-4200	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-t <sub>RCD</sub> -t <sub>RP</sub>	3-3-3	4-4-4	5-5-5	6-6-6

\* Consult factory for availability



## PIN CONFIGURATION

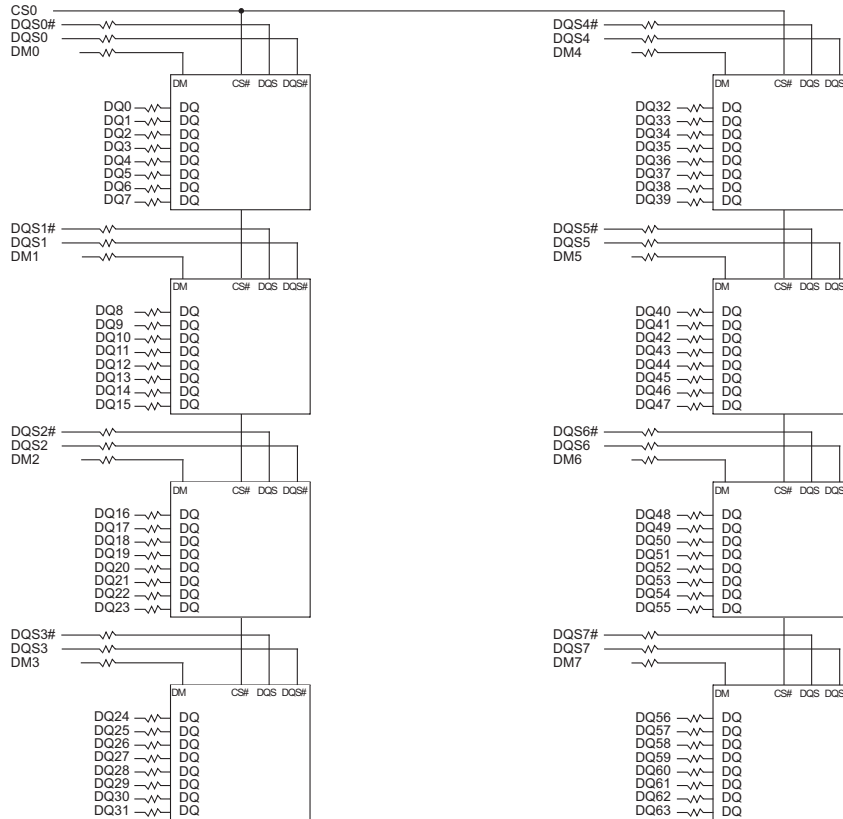
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	VREF	61	A4	121	Vss	181	Vccq
2	Vss	62	Vccq	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	Vcc	124	Vss	184	Vcc
5	Vss	65	Vss	125	DM0	185	CK0
6	DQS0#	66	Vss	126	NC	186	CK0#
7	DQS0	67	Vcc	127	Vss	187	Vcc
8	Vss	68	NC	128	DQ6	188	A0
9	DQ2	69	Vcc	129	DQ7	189	Vcc
10	DQ3	70	A10/AP	130	Vss	190	BA1
11	Vss	71	BA0	131	DQ12	191	Vccq
12	DQ8	72	Vccq	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	Vss	193	CS0#
14	Vss	74	CAS#	134	DM1	194	Vccq
15	DQS1#	75	Vccq	135	NC	195	ODT0
16	DQS1	76	NC	136	Vss	196	NC
17	Vss	77	NC	137	CK1	197	Vcc
18	NC	78	Vccq	138	CK1#	198	Vss
19	NC	79	Vss	139	Vss	199	DQ36
20	Vss	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	Vss
22	DQ11	82	Vss	142	Vss	202	DM4
23	Vss	83	DQS4#	143	DQ20	203	NC
24	DQ16	84	DQS4	144	DQ21	204	Vss
25	DQ17	85	Vss	145	Vss	205	DQ38
26	Vss	86	DQ34	146	DM2	206	DQ39
27	DQS2#	87	DQ35	147	NC	207	Vss
28	DQS2	88	Vss	148	Vss	208	DQ44
29	Vss	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	Vss
31	DQ19	91	Vss	151	Vss	211	DM5
32	Vss	92	DQS5#	152	DQ28	212	NC
33	DQ24	93	DQS5	153	DQ29	213	Vss
34	DQ25	94	Vss	154	Vss	214	DQ46
35	Vss	95	DQ42	155	DM3	215	DQ47
36	DQS3#	96	DQ43	156	NC	216	Vss
37	DQS3	97	Vss	157	Vss	217	DQ52
38	Vss	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	Vss
40	DQ27	100	Vss	160	Vss	220	CK2
41	Vss	101	SA2	161	NC	221	CK2#
42	NC	102	NC	162	NC	222	Vss
43	NC	103	Vss	163	Vss	223	DM6
44	Vss	104	DQS6#	164	NC	224	NC
45	NC	105	DQS6	165	NC	225	Vss
46	DQS8	106	Vss	166	Vss	226	DQ54
47	Vss	107	DQ50	167	NC	227	DQ55
48	NC	108	DQ51	168	NC	228	Vss
49	NC	109	Vss	169	Vss	229	DQ60
50	Vss	110	DQ56	170	Vccq	230	DQ61
51	Vccq	111	DQ57	171	NC	231	Vss
52	CKE0	112	Vss	172	Vcc	232	DM7
53	Vcc	113	DQS7#	173	NC	233	NC
54	NC	114	DQS7	174	NC	234	Vss
55	NC	115	Vss	175	Vccq	235	DQ62
56	Vccq	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	Vss
58	A7	118	Vss	178	Vcc	238	VCCSPD
59	Vcc	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

## PIN NAMES

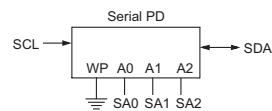
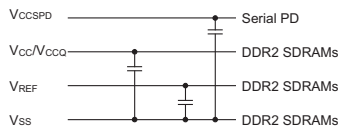
Pin Name	Function
A0-A12	Address Input
BA0, BA1	Bank Address
DQ0 ~ DQ63	Data Input/output
DQS0 ~ DQS7	Data Strobe
DQS0# ~ DQS7#	Data Strobe negative
ODT0	On Die Termination
CK0,CK0# - CK2, CK2#	Clock Input
CKE0	Clock enable input
CS0#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
Vcc	Voltage Supply (1.8V±0.1V)
Vccq	I/O Power (1.8V)
Vss	Ground
SA0 ~ SA2	SPD Address
SDA	Serial Data I/O
SCL	Serial clock
DM(0-7)	Data Masks
A10/AP	Address input/Auto precharge
VREF	I/O reference supply
VCCSPD	Serial EEPROM
NC	No Connect



**FUNCTIONAL BLOCK DIAGRAM**



- BA0-BA1 → BA0-BA1: DDR2 SDRAMs
- A0-A12 → A0-A12: DDR2 SDRAMs
- RAS# → RAS#: DDR2 SDRAMs
- CAS# → CAS#: DDR2 SDRAMs
- WE# → WE#: DDR2 SDRAMs
- CKE0 → CKE0: DDR2 SDRAMs
- ODT0 → ODT0: DDR2 SDRAMs



*Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	2 DDR2 SDRAMs
*CK1/CK1	3 DDR2 SDRAMs
*CK2/CK2	3 DDR2 SDRAMs

\*Wire per Clock Loading Table/Wiring Diagrams

- Notes:
1. DQ, DM, DQS/DQS# resistors: 5.1 Ohms +/-5%
  2. BAx, Ax, RAS#, CAS#, WE# resistors: 5.1 Ohms +/-5%

NOTE: All resistor values are 22 ohms unless otherwise specified.



### DC OPERATING CONDITIONS

All Voltages Referenced to V<sub>SS</sub>

Parameter	Symbol	Rating			Units	Notes
		Min.	Type	Max.		
Supply Voltage	V <sub>CC</sub>	1.7	1.8	1.9	V	1
I/O Supply Voltage	V <sub>CCQ</sub>	1.7	1.8	1.9	V	4
VCCL Supply Voltage	V <sub>CCL</sub>	1.7	1.8	1.9	V	4
I/O Reference Voltage	V <sub>REF</sub>	0.49*V <sub>CCQ</sub>	0.50*V <sub>CCQ</sub>	0.51*V <sub>CCQ</sub>	V	2
I/O Termination Voltage	V <sub>TT</sub>	V <sub>REF</sub> -0.04	V <sub>REF</sub>	V <sub>REF</sub> +0.04	V	3

**Notes:**

- V<sub>CC</sub> and V<sub>CCQ</sub> must track each other. V<sub>CCQ</sub> must be less than or equal to V<sub>CC</sub>.
- V<sub>REF</sub> is expected to equal V<sub>CCQ</sub>/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V<sub>REF</sub> may not exceed +/- percent of the DC value. Peak-to-peak AC noise on V<sub>REF</sub> may not exceed +/-2 percent of V<sub>REF</sub>. This measurement is to be taken at the nearest V<sub>REF</sub> bypass capacitor.
- V<sub>TT</sub> is not applied directly to the device. V<sub>TT</sub> is a system supply for signal termination resistors, is expected to be set equal to V<sub>REF</sub> and must track variations in the DC level of V<sub>REF</sub>.
- V<sub>CCQ</sub> tracks with V<sub>CC</sub>; V<sub>CCL</sub> track with V<sub>CC</sub>.

### ABSOLUTE MAXIMUM RATINGS

SSTL\_1.8V

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	Voltage on V <sub>CC</sub> pin relative to V <sub>SS</sub>	- 1.0	2.3	V	
V <sub>CCQ</sub>	Voltage on V <sub>CCQ</sub> pin relative to V <sub>SS</sub>	- 0.5	2.3	V	
V <sub>CCL</sub>	Voltage on V <sub>CCL</sub> pin relative to V <sub>SS</sub>	- 0.5	2.3	V	
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to V <sub>SS</sub>	- 0.5	2.3	V	
T <sub>STG</sub>	Storage Temperature	-55	100	°C	
T <sub>CASE</sub>	Device operating Temperature	0	85	°C	
I <sub>L</sub>	Input leakage current; Any input 0V<V <sub>IN</sub> <V <sub>CC</sub> ; V <sub>REF</sub> input 0V<V <sub>IN</sub> <<0.95; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#	-40	40	uA
		CS#, CKE	-40	40	uA
		CK, CK#	-15	15	uA
		DM	-5	5	uA
I <sub>OZ</sub>	Output leakage current; 0V<V <sub>OUT</sub> <V <sub>CCQ</sub> ; DQs and ODT are disable	-5	5	uA	
I <sub>VREF</sub>	V <sub>REF</sub> leakage current; V <sub>REF</sub> = Valid V <sub>REF</sub> level	-16	16	uA	



## CAPACITANCE

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ ,  $V_{CC} = V_{CCQ} = 1.8\text{V}$

Parameter	Symbol	Min	Max	Units
Input Capacitance: (A0 ~ A12, BA0 ~ BA1, RAS#, CAS#, WE#)	C <sub>IN1</sub>	12	20	pF
Input Capacitance: (CKE0), (ODT0)	C <sub>IN2</sub>	12	20	pF
Input Capacitance: (CS0#)	C <sub>IN3</sub>	12	20	pF
Input Capacitance: (CK0, CK0# ~ CK2, CK2#)	C <sub>IN4</sub>	7	10	pF
Input Capacitance: (DM0 ~ DM7)	C <sub>IN5</sub> (E6)	6.5	7.5	pF
	C <sub>IN6</sub> (D5)	6.5	8	pF
Input Capacitance: (DQ0 ~ DQ63)	C <sub>OUT1</sub> (E6)	6.5	7.5	pF
	C <sub>OUT1</sub> (D5)	6.5	8	pF

## OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating Temperature	TOPER	0°C to 85°C	°C	1, 2

Notes:

- Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2.
- At 0 - 85°C, operation temperature range, all DRAM specification will be supported.

## INPUT DC LOGIC LEVEL

All voltages referenced to V<sub>SS</sub>

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	V <sub>IH(DC)</sub>	VREF + 0.125	VREF + 0.300	V
Input Low (Logic 0) Voltage	V <sub>IL(DC)</sub>	-0.300	VREF - 0.125	V

## INPUT AC LOGIC LEVEL

All voltages referenced to V<sub>SS</sub>

Parameter	Symbol	Min	Max	Units
AC Input High (Logic 1) Voltage	V <sub>IH(AC)</sub>	VREF + 0.250		V
AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V <sub>IL(AC)</sub>		VREF - 0.250	V
AC Input Low (Logic 0) Voltage DDR2-667, DDR2-800 (TBD)	V <sub>IL(AC)</sub>		VREF - 0.200	V



### DDR2 Icc SPECIFICATIONS AND CONDITIONS

Symbol	Proposed Conditions	806	665	534	403	Units	
Icc0*	Operating one bank active-precharge current; tCK = tCK(Icc), tRC = tRC(Icc), tRAS = tRASmin(Icc); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	840	800	760	mA	
Icc1*	Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(Icc), AL = 0; tCK = tCK(Icc), tRC = tRC(Icc), tRAS = tRASmin(Icc), tRCD = tRCD(Icc); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as Icc4W	TBD	920	880	800	mA	
Icc2P**	Precharge power-down current; All banks idle; tCK = tCK(Icc); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	64	64	64	mA	
Icc2Q**	Precharge quiet standby current; All banks idle; tCK = tCK(Icc); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	240	200	200	mA	
Icc2N**	Precharge standby current; All banks idle; tCK = tCK(Icc); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	280	240	240	mA	
Icc3P**	Active power-down current; All banks open; tCK = tCK(Icc); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	280	240	240	mA
		Slow PDN Exit MRS(12) = 1	TBD	120	120	120	mA
Icc3N**	Active standby current; All banks open; tCK = tCK(Icc), tRC = tRC(Icc), tRAS = tRASmin(Icc); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	600	560	520	mA	
Icc4W**	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(Icc), AL = 0; tCK = tCK(Icc), tRAS = tRASmax(Icc), tRP = tRP(Icc); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	1680	1400	1080	mA	
Icc4R*	Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(Icc), AL = 0; tCK = tCK(Icc), tRAS = tRASmax(Icc), tRP = tRP(Icc); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as Icc4W	TBD	1480	1280	1040	mA	
Icc5B**	Burst auto refresh current; tCK = tCK(Icc); Refresh command at every tRFC(Icc) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	1360	1320	1280	mA	
Icc6*	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	TBD	40	40	40	mA
Icc7*	Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(Icc), AL = tRCD(Icc)-1*tCK(Icc); tCK = tCK(Icc), tRC = tRC(Icc), tRRD = tRRD(Icc), tRCD = 1*tCK(Icc); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are switching.	TBD	2120	2040	2040	mA	

\* Value calculated as one module rank in the operating condition, and all other module ranks in Icc2P (CKE LOW) mode.

\*\* Value calculated reflects all module ranks in this operating condition

NOTES:

- Icc specifications were calculated using **SAMSUNG** components. Other manufactures DRAMs may have different values.



**AC TIMING PARAMETERS**

0°C ≤ T<sub>case</sub> < +85°C; V<sub>CCQ</sub> = + 1.8V ± 0.1V, V<sub>CC</sub> = +1.8V ± 0.1V

AC CHARACTERISTICS			806		665		534		403			
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 6	t <sub>CK(6)</sub>	TBD	TBD							ps
		CL = 5	t <sub>CK(5)</sub>	TBD	TBD	3,000	8,000					ps
		CL = 4	t <sub>CK(4)</sub>	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	t <sub>CK(3)</sub>	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width		t <sub>CH</sub>	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>
	CK low-level width		t <sub>CL</sub>	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>
	Half clock period		t <sub>HP</sub>	TBD	TBD	MIN (t <sub>CH</sub> , t <sub>CL</sub> )		MIN (t <sub>CH</sub> , t <sub>CL</sub> )		MIN (t <sub>CH</sub> , t <sub>CL</sub> )		ps
Data	DQ output access time from CK/CK#		t <sub>AC</sub>	TBD	TBD	-450	+450	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t <sub>HZ</sub>	TBD	TBD		t <sub>AC</sub> (MAX)		t <sub>AC</sub> (MAX)		t <sub>AC</sub> (MAX)	ps
	Data-out low-impedance window from CK/CK#		t <sub>LZ</sub>	TBD	TBD	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)	ps
	DQ and DM input setup time relative to DQS		t <sub>DS</sub>	TBD	TBD	100		100		150		ps
	DQ and DM input hold time relative to DQS		t <sub>DH</sub>	TBD	TBD	225		225		275		ps
	A DQ and DM input pulse width (for each input)		t <sub>DIPW</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>
	Data hold skew factor		t <sub>QHS</sub>	TBD	TBD		340		400		450	ps
	DQ...DQS hold, DQS to first DQ to go nonvalid, per access		t <sub>QH</sub>	TBD	TBD	t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>HP</sub> - t <sub>QHS</sub>		ps
Data valid output window (DVW)		t <sub>DVW</sub>	TBD	TBD	t <sub>QH</sub> - t <sub>DQSQ</sub>		t <sub>QH</sub> - t <sub>DQSQ</sub>		t <sub>QH</sub> - t <sub>DQSQ</sub>		ns	
Data Strobe	DQS input high pulse width		t <sub>DQSH</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>
	DQS input low pulse width		t <sub>DQSL</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>
	DQS output access time from CK/CK#		t <sub>DQSC</sub>	TBD	TBD	-400	+400	-450	+450	-500	+500	ps
	DQS falling edge to CK rising ... setup time		t <sub>DSS</sub>	TBD	TBD	0.2		0.2		0.2		t <sub>CK</sub>
	DQS falling edge from CK rising ... hold time		t <sub>DSH</sub>	TBD	TBD	0.2		0.2		0.2		t <sub>CK</sub>
	DQS...DQ skew, DQS to last DQ valid, per group, per access		t <sub>DQSQ</sub>	TBD	TBD		240		300		350	ps
	DQS read preamble		t <sub>RPRE</sub>	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t <sub>CK</sub>
	DQS read postamble		t <sub>RPST</sub>	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>
	DQS write preamble setup time		t <sub>WPRES</sub>	TBD	TBD	0		0		0		ps
	DQS write preamble		t <sub>WPRE</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>
	DQS write postamble		t <sub>WPST</sub>	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>
	Write command to first DQS latching transition		t <sub>DQSS</sub>	TBD	TBD	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t <sub>CK</sub>
Address and control input pulse width for each input		t <sub>IPW</sub>	TBD	TBD	0.6		0.6		0.6		t <sub>CK</sub>	

NOTE:

• AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

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**AC TIMING PARAMETERS (cont'd)**

0°C ≤ T<sub>case</sub> < +85°C; V<sub>CCQ</sub> = + 1.8V ± 0.1V, V<sub>CC</sub> = +1.8V ± 0.1V

AC CHARACTERISTICS			806		665		534		403		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	Address and control input setup time	t <sub>IS</sub>	TBD	TBD	200		250		250		ps
	Address and control input hold time	t <sub>IH</sub>	TBD	TBD	275		375		475		ps
	CAS# to CAS# command delay	t <sub>CCD</sub>	TBD	TBD	2		2		2		tck
	ACTIVE to ACTIVE (same bank) command	t <sub>RC</sub>	TBD	TBD	54		55		55		ns
	ACTIVE bank a to ACTIVE bank b command	t <sub>RRD</sub>	TBD	TBD	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t <sub>RCd</sub>	TBD	TBD	15		15		15		ns
	Four Bank Activate period	t <sub>FAW</sub>	TBD	TBD	37.5	37.5	37.5	37.5	37.5	37.5	
	ACTIVE to PRECHARGE command	t <sub>RAS</sub>	TBD	TBD	45	70,000	45	70,000	45	70,000	ns
	Internal READ to precharge command delay	t <sub>RTP</sub>	TBD	TBD	7.5		7.5		7.5		ns
	Write recovery time	t <sub>WR</sub>	TBD	TBD	15		15		15		ns
	Auto precharge write recovery + precharge time	t <sub>DAL</sub>	TBD	TBD	t <sub>WR</sub> + t <sub>RP</sub>		t <sub>WR</sub> + t <sub>RP</sub>		t <sub>WR</sub> + t <sub>RP</sub>		ns
	Internal WRITE to READ command delay	t <sub>WTR</sub>	TBD	TBD	10		7.5		10		ns
	PRECHARGE command period	t <sub>RP</sub>	TBD	TBD	15		15		15		
	PRECHARGE ALL command period	t <sub>RPA</sub>	TBD	TBD	t <sub>WR</sub> + t <sub>CK</sub>		t <sub>WR</sub> + t <sub>CK</sub>		t <sub>WR</sub> + t <sub>CK</sub>		ns
LOAD MODE command cycle time	t <sub>MRD</sub>	TBD	TBD	2		2		2		tck	
CKE low to CK,CK# uncertainty	t <sub>DELAY</sub>	TBD	TBD	t <sub>IS</sub> + t <sub>CK</sub> + t <sub>IH</sub>		t <sub>IS</sub> + t <sub>CK</sub> + t <sub>IH</sub>		t <sub>IS</sub> + t <sub>CK</sub> + t <sub>IH</sub>		ns	
Refresh	REFRESH to REFRESH command interval	t <sub>RFC</sub>	TBD	TBD	127.5	70,000	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t <sub>REFI</sub>	TBD	TBD		7.8		7.8		7.8	μs
Self Refresh	Exit self refresh to non-READ command	t <sub>XSNR</sub>	TBD	TBD	t <sub>RFC</sub> (MIN) + 10		t <sub>RFC</sub> (MIN) + 10		t <sub>RFC</sub> (MIN) + 10		ns
	Exit self refresh to READ command	t <sub>XSRD</sub>	TBD	TBD	200		200		200		tck
	Exit self refresh timing reference	t <sub>ISXR</sub>	TBD	TBD	t <sub>IS</sub>		t <sub>IS</sub>		t <sub>IS</sub>		ps
ODT	ODT turn-on delay	t <sub>AOND</sub>	TBD	TBD	2	2	2	2	2	2	tck
	ODT turn-on	t <sub>AON</sub>	TBD	TBD	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 1000	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 1000	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 1000	ps
	ODT turn-off delay	t <sub>AOFD</sub>	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	tck
	ODT turn-off	t <sub>AOF</sub>	TBD	TBD	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 600	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 600	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 600	ps
	ODT turn-on (power-down mode)	t <sub>AONPD</sub>	TBD	TBD	t <sub>AC</sub> (MIN) + 2000	2 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1000	t <sub>AC</sub> (MIN) + 2000	2 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1000	t <sub>AC</sub> (MIN) + 2000	2 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t <sub>AOFPD</sub>	TBD	TBD	t <sub>AC</sub> (MIN) + 2000	2.5 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1000	t <sub>AC</sub> (MIN) + 2000	2.5 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1000	t <sub>AC</sub> (MIN) + 2000	2.5 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1000	ps
	ODT to power-down entry latency	t <sub>ANPD</sub>	TBD	TBD	3		3		3		tck
	ODT power-down exit latency	t <sub>AXPD</sub>	TBD	TBD	8		8		8		tck
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t <sub>XARD</sub>	TBD	TBD	2		2		2		tck
	Exit active power-down to READ command, MR[bit12=1]	t <sub>XARDS</sub>	TBD	TBD	7 - AL		6 - AL		6 - AL		tck
	A Exit precharge power-down to any non-READ command.	t <sub>XP</sub>	TBD	TBD	2		2		2		tck
	CKE minimum high/low time	t <sub>CKE</sub>	TBD	TBD	3		3		3		tck

NOTE:

- AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.





### ORDERING INFORMATION FOR D6

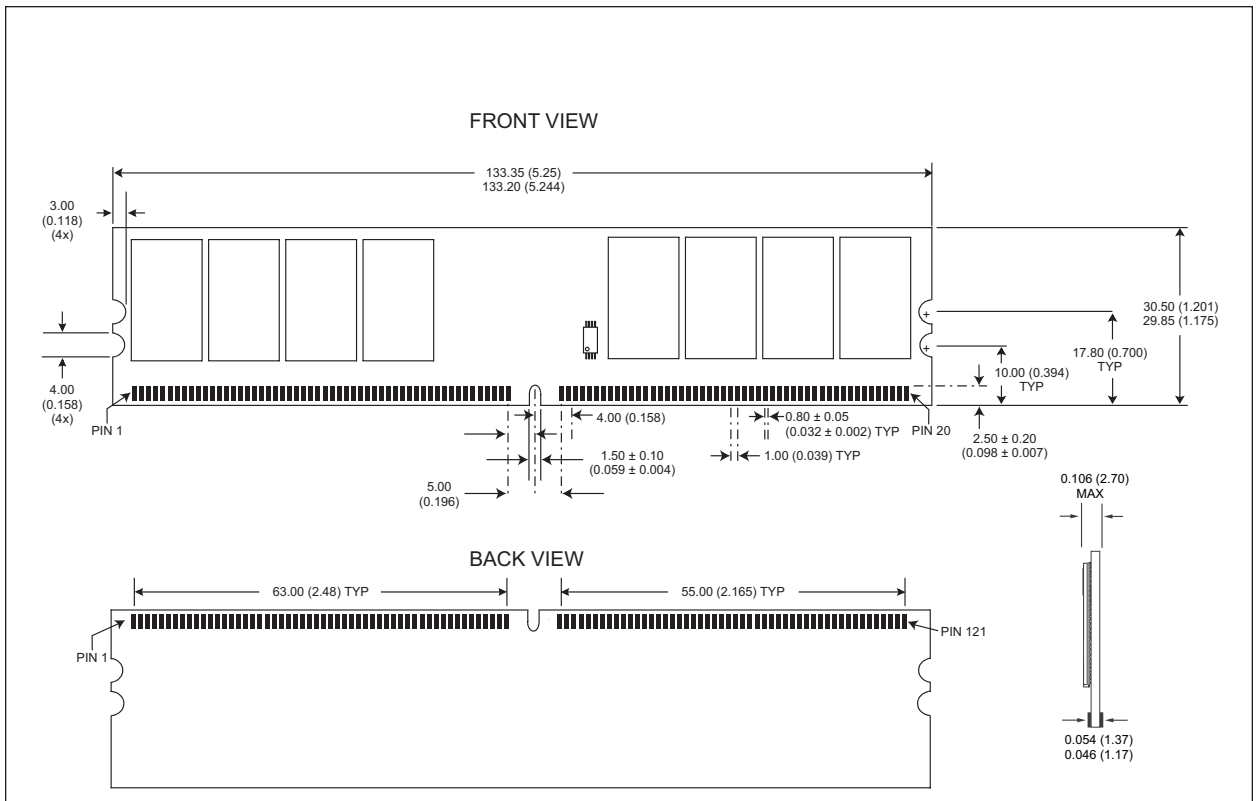
Part Number	Speed/Data Rate	CAS Latency	t <sub>RC</sub> D	t <sub>RP</sub>	Height*
WV3HG32M64EEU806D6xG**	400MHz/800Mb/s	6	6	6	30.00mm (1.181") TYP
WV3HG32M64EEU665D6xG**	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG32M64EEU534D6xG	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG32M64EEU403D6xG	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

\*\* Consult factory for availability

#### NOTES:

- RoHS compliant product. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (G = Infineon, M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

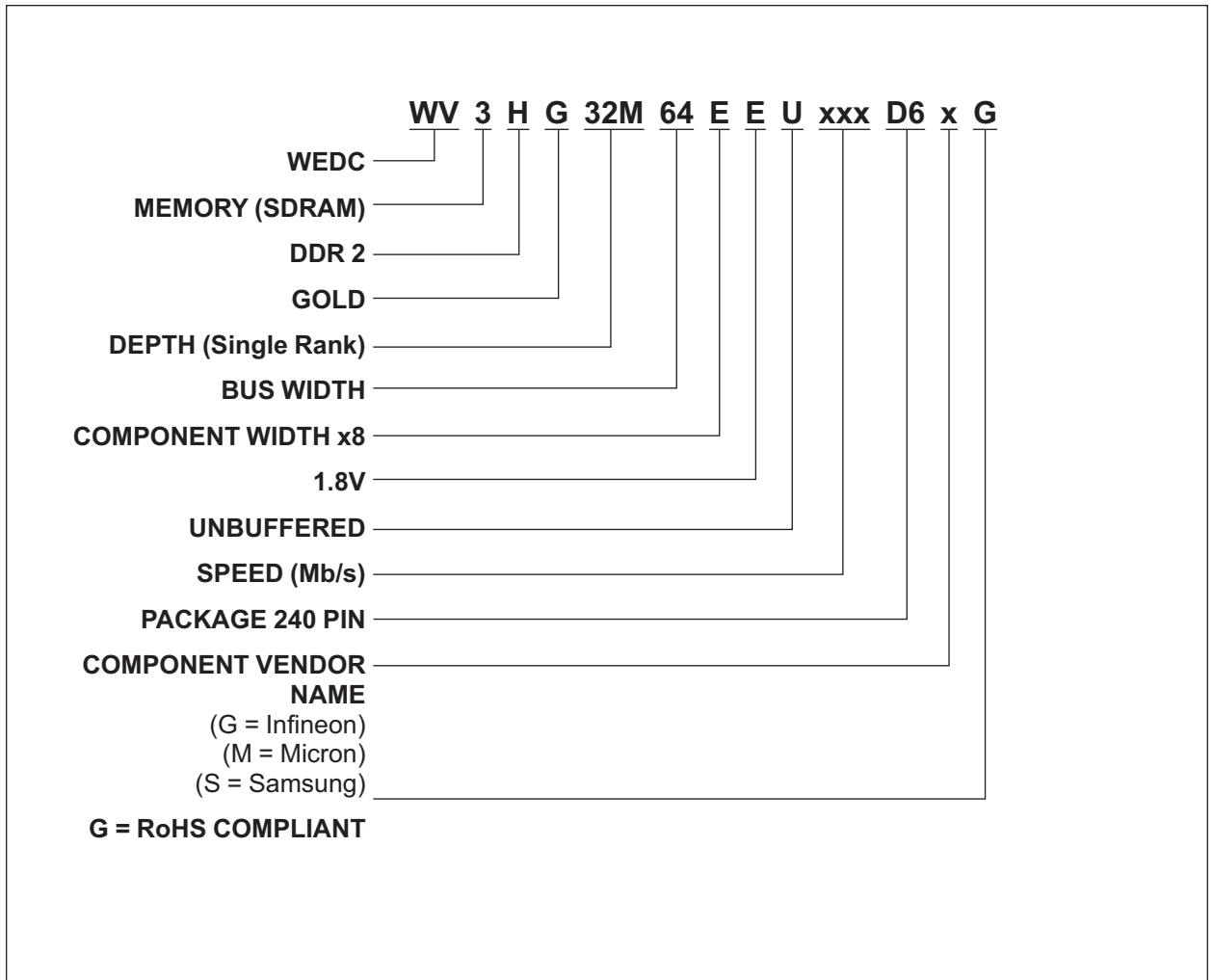
### PACKAGE DIMENSIONS FOR D6



\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



**PART NUMBERING GUIDE**





**Document Title**

256MB – 32Mx64 DDR2 SDRAM UNBUFFERED

**Revision History**

<b>Rev #</b>	<b>History</b>	<b>Release Date</b>	<b>Status</b>
Rev 0	Created	December 2005	Advanced