

Actual Size = 3.2 x 2.5mm



Product Features

- Less than 1.5 ps RMS jitter with fundamental or overtone design
- 1.8V CMOS compatible logic levels
- Pin-compatible with standard 3.2x2.5mm packages
- Designed for standard reflow and washing techniques
- Low power standby mode: 10 uA max
- Pb-free and RoHS/Green compliant

Product Description

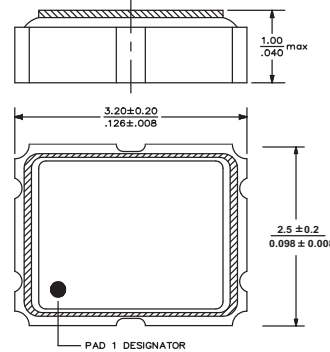
The S1642 Series is a 1.8V crystal clock oscillator that achieves superb jitter and stability over a broad range of operating conditions and frequencies. The output clock signal, generated internally with a non-PLL oscillator design, is compatible with LVCMOS logic levels. The device, available on tape and reel, is contained in a 3.2x2.5mm surface-mount ceramic package.

Applications

The S1642 Series is an ideal reference clock for compact, high-density applications requiring low jitter tight stability, or low power consumption, including:

- WLAN
- HBA
- Portable Multimedia Player (PMP)
- Notebook Computer
- SDIO / PCMCIA CARD
- USB BT Interface
- Bluetooth

Packaging Outline



Pin Functions

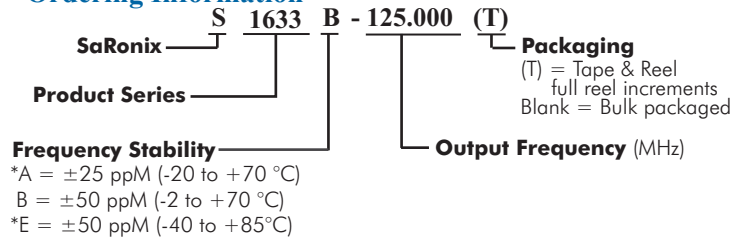
Pin	Function
1	OE Function
2	Ground
3	Clock Output
4	V _{DD}

Common Frequencies

Contact SaRonix for additional frequencies

10.0000 MHz	24.5760 MHz	48.0000 MHz
14.3181 MHz	25.0000 MHz	66.0000 MHz
16.0000 MHz	27.0000 MHz	75.0000 MHz
20.0000 MHz	32.0000 MHz	
24.0000 MHz	40.0000 MHz	

Ordering Information



* Availability varies by frequency.

Electrical Performance

Parameter	Min.	Typ.	Max.	Units	Notes
Output frequency	1.5440		100	MHz	As specified
Supply voltage	1.71	1.8	1.89	V	
Supply current, output enabled			4	mA	1.5440 to <36 MHz
			7		36 to <50 MHz
			10		50 to <70 MHz
			20		70 to 100 MHz
Standby current			10	μA	1.5440 to <36MHz
			100	uA	36 to 100MHz
Frequency stability			±25 to ±50	ppM	See Note 1 below
Operating temperature	-40		+85	°C	As specified
Output logic 0, VOL			10% V _{DD}	V	
Output logic 1, VOH	90% V _{DD}			V	
Output load	15 pF (max)				
Duty cycle	45		55	%	measured 50%VDD
Rise and fall time	<36 MHz		4	ns	measured 20/80% of waveform
	36 to 100 MHz		2.5		
Jitter, Phase	up to 75 MHz		1.5	ps RMS (1-σ)	10kHz to 20 MHz frequency band
	75 to 100 MHz		1		
Jitter, Accumulated	up to <75 MHz		5	ps RMS (1-σ)	20.000 adjacent periods
	75 to 100 MHz		3		
Jitter, Total	up to <75 MHz		50	ps pk-pk	100.000 random periods
	75 to 100 MHz		30		

Notes:

- As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (1 year at 25°C average effective ambient temperature), shock and vibration.

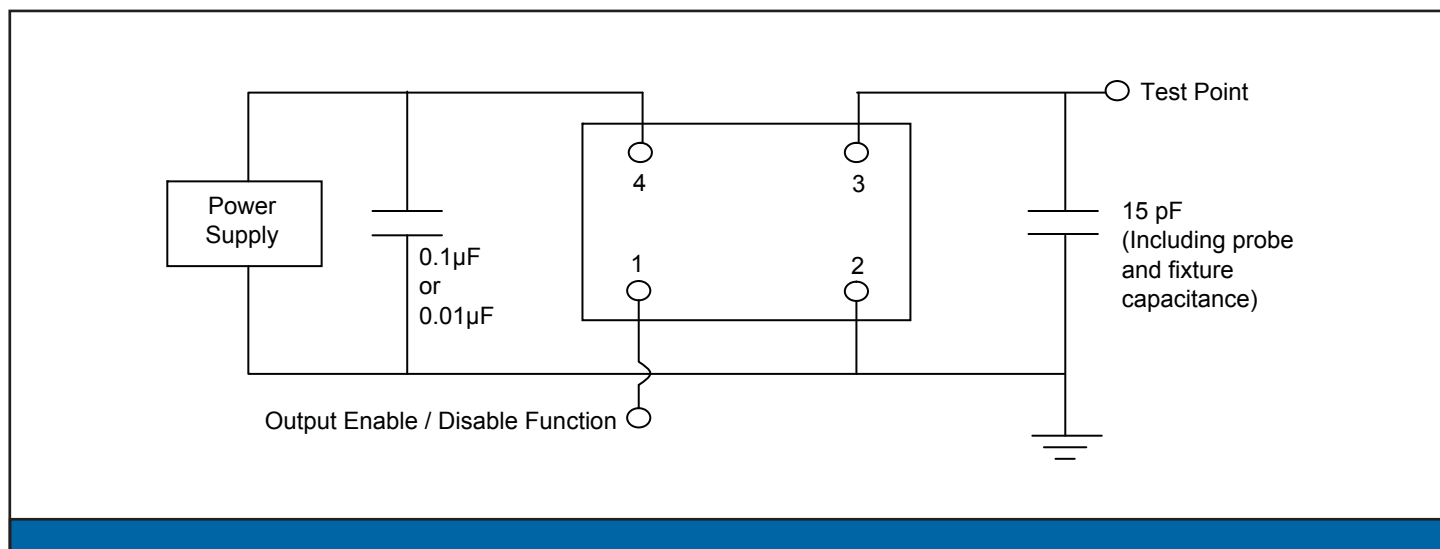
Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	0.7 V _{DD}			V	or open
Input voltage (pin 1), Output Disable (low power standby)			0.3 V _{DD}	V	Output is Hi-Z
Internal pullup resistance	30			kΩ	
Output disable delay			200	ns	
Output enable delay			10	ms	

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	

Test Circuit

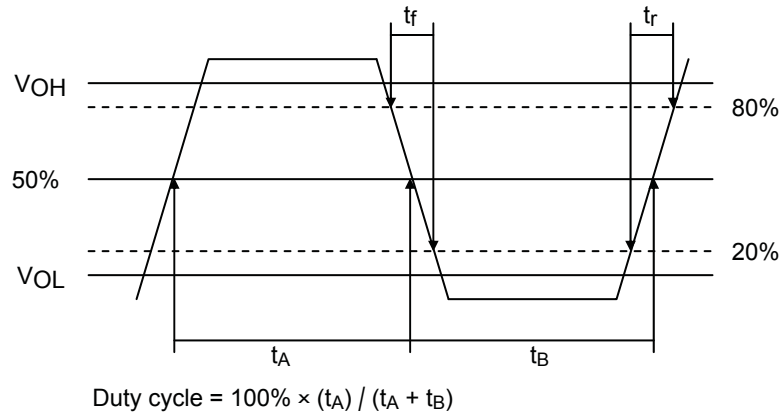


Reliability Test Ratings

This product is rated to meet the following test conditions:

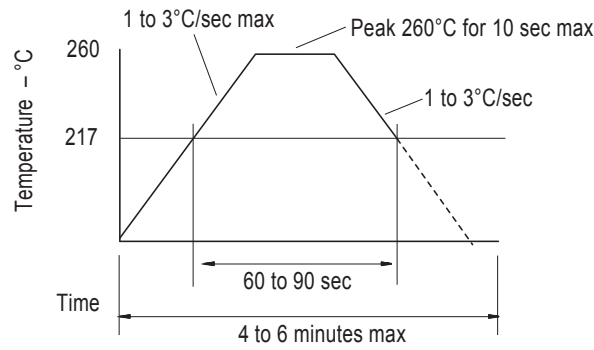
Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2 \times 10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

Output Waveform

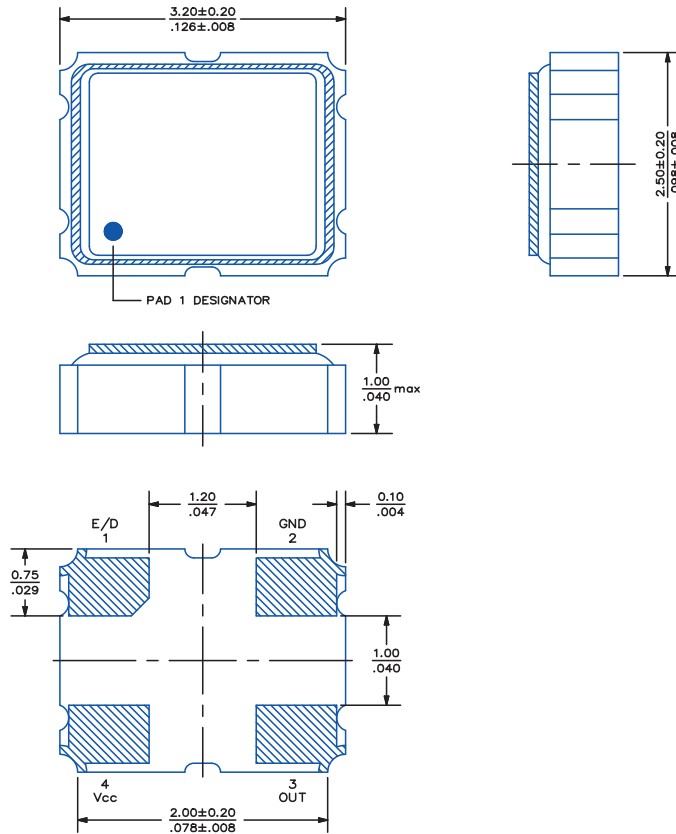


Reflow Soldering Profile

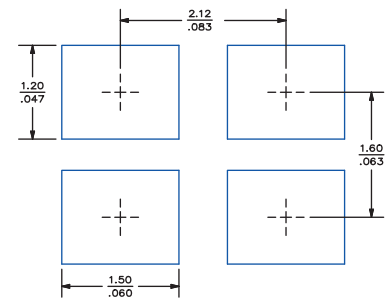
As per IPC/JEDEC J-STD-020C



Mechanical Drawings



Recommended Land Pattern*



*External high-frequency power decoupling is recommended.(see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions are in mm/inches.

Marking LINE 1: S12.3456 (SaRonix, Frequency Code)
Marking LINE 2: ● YY WW X2X (Pin 1, Year, Week, Origin, Model, Internal Use)

**Exact location of markings may vary.