



Mobile Double Data Rate (DDR) SDRAM

MT46H8M16LF – 2 Meg x 16 x 4 Banks

For a complete data sheet, please refer to www.micron.com/mobilesds.

Features

- VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data masks (DM) for masking write data—one mask per byte
- Programmable burst lengths: 2, 4, or 8
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS compatible inputs
- On-chip temperature sensor to control refresh rate
- Partial array self refresh (PASR)
- Selectable output drive (DS)
- Clock stop capability

Options

- VDD/VDDQ
 - 1.8V/1.8V
- Configuration
 - 8 Meg x 16 (2 Meg x 16 x 4 banks)
- Plastic Package
 - 60-Ball VFBGA (Lead-Free)
- Timing – Cycle Time
 - 7.5ns @ CL = 3
 - 10ns @ CL = 3
- Operating Temperature Range
 - Commercial (0° to +70°C)
 - Industrial (-40°C to +85°C)

Marking

H
8M16
CF
-6
-10
None
IT

Figure 1: 60-Ball VFBGA Assignment (Top View)

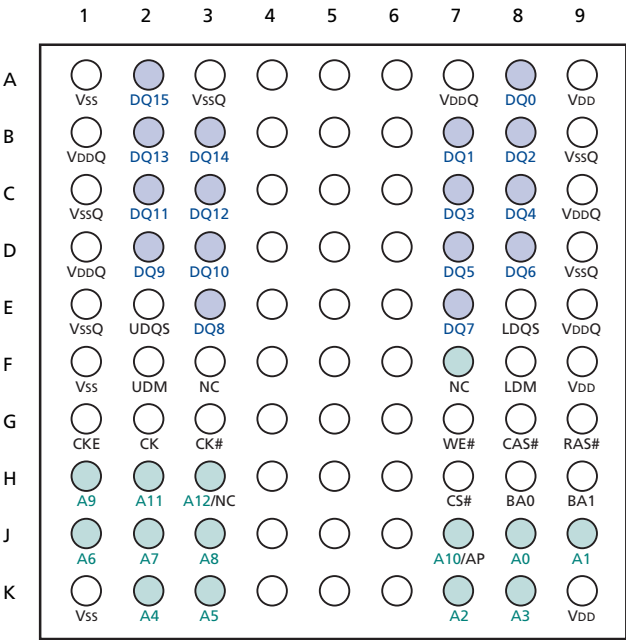


Table 1: Configuration Addressing

Architecture	8 Meg x 16
Configuration	2 Meg x 16 x 4
Refresh Count	4K
Row Addressing	4K (A0–A11)
Bank Addressing	4 (BA0, BA1)
Column Addressing	1K (A0–A9)

Table 2: Key Timing Parameters

Speed Grade	Clock Rate		Data-Out Window	Access Time	DQS-DQ Skew
	CL = 3	CL = 2			
-75	133 MHz	-	2ns	6.0s	+0.6ns
-10	104 MHz	-	2.8ns	7.0ns	+0.7ns
-75	-	83 MHz	4ns	6.5ns	+0.6ns
-10	-	67 MHz	5ns	7.0ns	+0.7ns



128Mb: 8 Meg x 16 Mobile DDR SDRAM



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Advance: This data sheet contains initial descriptions of products still under development.**



Revision History

- Original Document, Advance03/05