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100180

High Speed 8–Bit Adder

FEATURES

- **Typical propagation delay: 2.35ns**
- **Typical supply current ($-I_{EE}$): 205mA**

DESCRIPTION

The 100180 is a high–speed adder that can add two six–bit operands (A_n, B_n) and an Active–Low carry input ($\overline{C}_{IN}$).

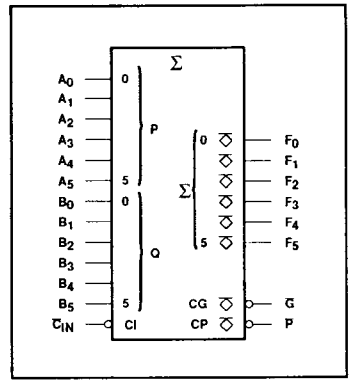
The sum is presented on the function outputs (F_n). When used in conjuction with the 100179, the carry generate and propagate outputs ($\overline{G}$ and $\overline{P}$) allow more than one 100180 to add operands larger than 6–bits.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_5$	Operand A Inputs
$B_0 - B_5$	Operand B Inputs
$\overline{C}_{IN}$	Carry Input (Active–Low)
$\overline{G}$	Carry Generate Output (Active–Low)
$\overline{P}$	Carry Propagate Output (Active–Low)
$F_0 - F_5$	Function Outputs

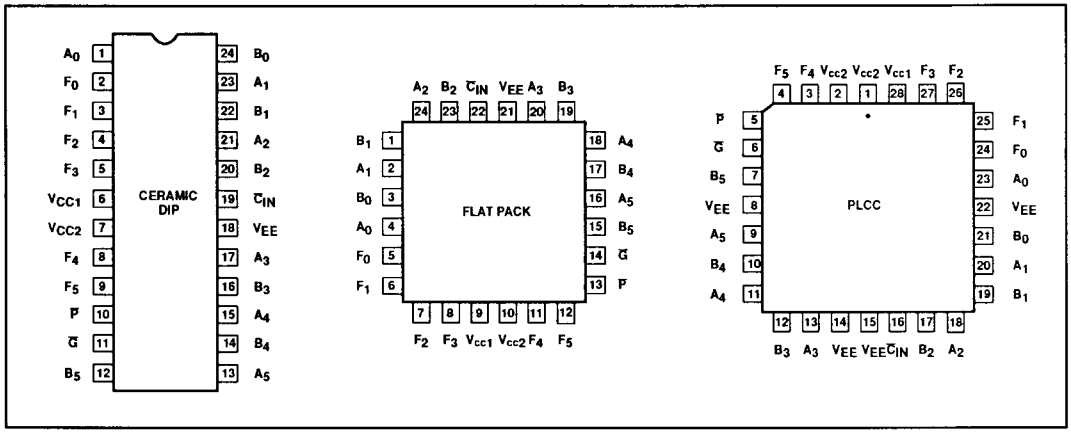
IEC/IEEE SYMBOL



ORDERING INFORMATION

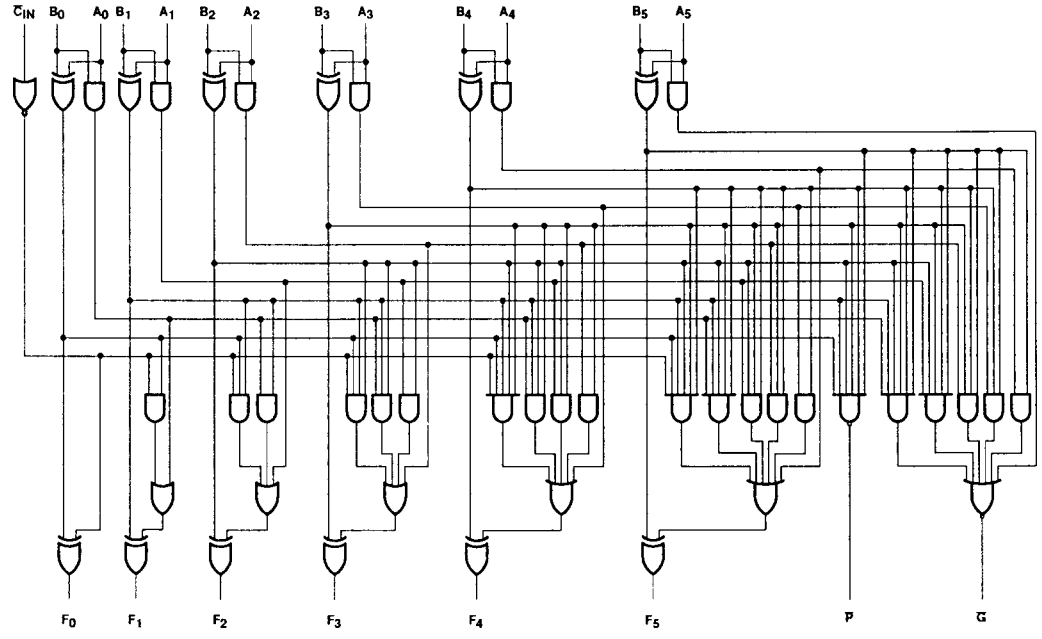
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100180F
24–Pin Ceramic Flat Pack	100180Y
28–Pin PLCC	100180A

PIN CONFIGURATIONS



Adder 100180

LOGIC DIAGRAM



LOGIC EQUATIONS

$P_i = A_i \oplus B_i$

$G_i = A_i B_i$

$i = 0, 1, 2, 3, 4, 5$

$F_0 = P_0 \oplus C_{IN}$

$F_1 = P_1 \oplus (G_0 + P_0 C_{IN})$

$F_2 = P_2 \oplus (G_1 + P_1 G_0 + P_1 P_0 C_{IN})$

$F_3 = P_3 \oplus (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{IN})$

$F_4 = P_4 \oplus (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_{IN})$

$F_5 = P_5 \oplus (G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 G_0 + P_4 P_3 P_2 P_1 P_0 C_{IN})$

$\overline{P} = \overline{P_0 P_1 P_2 P_3 P_4 P_5}$

$\overline{G} = \overline{G_5 + P_5 G_4 + P_5 P_4 G_3 + P_5 P_4 P_3 G_2 + P_5 P_4 P_3 P_2 G_1 + P_5 P_4 P_3 P_2 P_1 G_0}$

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electyrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					220	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}.			135	205	290	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C MIN.	LIMITS T_A = 0°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10	4.70	1.10	4.60	1.10	4.70	ns
t_{PHL}			1.10	4.70	1.10	4.60	1.10	4.70	ns
t_{PLH}	Propagation delay A_n, B_n to $\overline{P}$		1.00	3.00	1.00	3.00	1.00	3.30	ns
t_{PHL}			1.00	3.00	1.00	3.00	1.00	3.30	ns
t_{PLH}	Propagation delay A_n, B_n to $\overline{G}$		1.10	3.90	1.20	3.80	1.20	3.90	ns
t_{PHL}			1.10	3.90	1.20	3.80	1.20	3.90	ns
t_{PLH}	Propagation delay $\overline{C}_{IN}$ to F_n		0.90	4.00	0.90	3.90	0.90	4.00	ns
t_{PHL}			0.90	4.00	0.90	3.90	0.90	4.00	ns
t_{TLH}	Transition time F_n, $\overline{P}$, $\overline{G}$		0.45	2.30	0.45	2.20	0.45	2.30	ns
t_{THL}			0.45	2.30	0.45	2.20	0.45	2.30	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10 1.10	4.70 4.70	1.10 1.10	4.60 4.60	1.10 1.10	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$		1.00 1.00	3.00 3.00	1.00 1.00	3.00 3.00	1.00 1.00	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{G}$		1.10 1.10	3.90 3.90	1.20 1.20	3.80 3.80	1.20 1.20	3.90 3.90	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		0.90 0.90	4.00 4.00	0.90 0.90	3.90 3.90	0.90 0.90	4.00 4.00	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{P}$, $\overline{G}$		0.45 0.45	2.30 2.30	0.45 0.45	2.20 2.20	0.45 0.45	2.30 2.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10 1.10	4.50 4.50	1.10 1.10	4.40 4.40	1.10 1.10	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$		1.00 1.00	2.80 2.80	1.00 1.00	2.80 2.80	1.00 1.00	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{G}$		1.10 1.10	3.70 3.70	1.20 1.20	3.60 3.60	1.20 1.20	3.70 3.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		0.90 0.90	3.80 3.80	0.90 0.90	3.70 3.70	0.90 0.90	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{P}$, $\overline{G}$		0.45 0.45	2.30 2.30	0.45 0.45	2.20 2.20	0.45 0.45	2.30 2.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

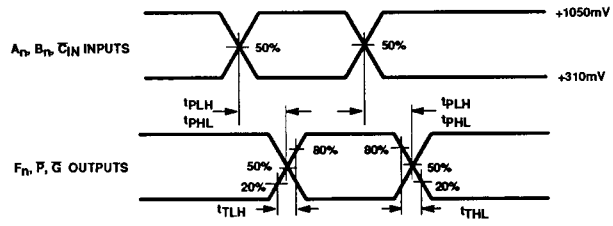
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10 1.10	4.50 4.50	1.10 1.10	4.40 4.40	1.10 1.10	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$		1.00 1.00	2.80 2.80	1.00 1.00	2.80 2.80	1.00 1.00	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{G}$		1.10 1.10	3.70 3.70	1.20 1.20	3.60 3.60	1.20 1.20	3.70 3.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		0.90 0.90	3.80 3.80	0.90 0.90	3.70 3.70	0.90 0.90	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{P}$, $\overline{G}$		0.45 0.45	2.30 2.30	0.45 0.45	2.20 2.20	0.45 0.45	2.30 2.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.