DDR SDRAM DIMM

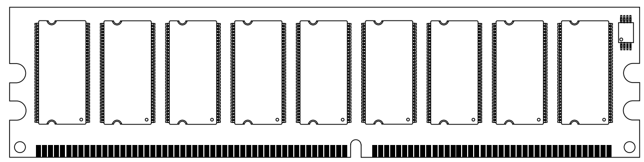
MT9VDDT1672A - 128MB
MT9VDDT3272A - 256MB

For the latest data sheet, please refer to the Micron® Web site: www.micron.com/moduleds

Features

- JEDEC-standard 184-pin dual in-line memory module (DIMM)
- Fast data transfer rates PC1600, PC2100, or PC2700
- Utilizes 200 MT/s, 266 MT/s, and 333MT/s DDR SDRAM components
- ECC-optimized pinout 128MB (16 Meg x 72), 256MB (32 Meg x 72)
- VDD= VDDQ= +2.5V
- VDDSPD = +2.3V to +3.6V
- +2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6µs (128MB), 7.8125µs (256MB) maximum average periodic refresh interval
- Serial Presence-Detect (SPD) with EEPROM
- Programmable READ CAS latency

Figure 1: 184-Pin DIMM (MO-206)



OPTIONS	MARKING
• Package	
Unbuffered	A
184-pin DIMM (Gold)	G
184-pin DIMM (Lead-Free)	Y
• Frequency/CAS Latency	
6ns, 333 MT/s (167 MHz), CL = 2.5	-335
7.5ns, 266 MT/s (133 MHz), CL = 2	-262
7.5ns, 266 MT/s (133 MHz), CL = 2	-26A
7.5ns, 266 MT/s (133 MHz), CL = 2.5	-265
10ns, 200 MT/s (100 MHz), CL = 2	-202
• Self Refresh	
Standard	None
Low Power	L

Table 1: Address Table

	128MB	256MB
Refresh Count	4K	8K
Row Addressing	4K (A0–A11)	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	16 Meg x 8	32 Meg x 8
Column Addressing	1K (A0–A9)	1K (A0–A9)
Module Rank Addressing	1 (S0#)	1 (S0#)

Table 2: Part Numbers and Timing Parameters

PART NUMBER	MODULE DENSITY	CONFIGURATION	MODULE BANDWIDTH	MEMORY CLOCK/ DATA RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)
MT9VDDT1672A(L)G-335__	128MB	16 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT9VDDT1672A(L)Y-335__	128MB	16 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT9VDDT1672A(L)G-262__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT9VDDT1672A(L)Y-262__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT9VDDT1672A(L)G-26A__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT1672A(L)Y-26A__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT1672A(L)G-265__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT9VDDT1672A(L)Y-265__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT9VDDT1672A(L)G-202__	128MB	16 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT9VDDT1672A(L)Y-202__	128MB	16 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT9VDDT3272A(L)G-335__	256MB	32 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT9VDDT3272A(L)Y335__	256MB	32 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT9VDDT3272A(L)G-262__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT9VDDT3272A(L)Y-262__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT9VDDT3272A(L)G-26A__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT3272A(L)Y-26A__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT3272A(L)G-265__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT9VDDT3272A(L)Y-265__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT9VDDT3272A(L)G-202__	256MB	32 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT9VDDT3272A(L)Y-202__	256MB	32 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2

NOTE:

All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9VDDT3272AG-265A1

Table 3: Pin Assignment (184-Pin DIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	24	DQ17	47	DQS8	70	VDD
2	DQ0	25	DQS2	48	A0	71	NC
3	VSS	26	VSS	49	CB2	72	DQ48
4	DQ1	27	A9	50	VSS	73	DQ49
5	DQS0	28	DQ18	51	CB3	74	VSS
6	DQ2	29	A7	52	BA1	75	CK2#
7	VDD	30	VDD	53	DQ32	76	CK2
8	DQ3	31	DQ19	54	VDD	77	VDD
9	NC	32	A5	55	DQ33	78	DQS6
10	NC	33	DQ24	56	DQS4	79	DQ50
11	VSS	34	VSS	57	DQ34	80	DQ51
12	DQ8	35	DQ25	58	VSS	81	VSS
13	DQ9	36	DQS3	59	BA0	82	NC
14	DQS1	37	A4	60	DQ35	83	DQ56
15	VDD	38	VDD	61	DQ40	84	DQ57
16	CK1	39	DQ26	62	VDD	85	VDD
17	CK1#	40	DQ27	63	WE#	86	DQS7
18	VSS	41	A2	64	DQ41	87	DQ58
19	DQ10	42	VSS	65	CAS#	88	DQ59
20	DQ11	43	A1	66	VSS	89	VSS
21	CKE0	44	CB0	67	DQS5	90	NC
22	VDD	45	CB1	68	DQ42	91	SDA
23	DQ16	46	VDD	69	DQ43	92	SCL

Table 4: Pin Assignment (184-Pin DIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
93	VSS	116	VSS	139	VSS	162	DQ47
94	DQ4	117	DQ21	140	DQS17	163	NC
95	DQ5	118	A11	141	A10	164	VDD
96	VDD	119	DQS11	142	CB6	165	DQ52
97	DQS9	120	VDD	143	VDD	166	DQ53
98	DQ6	121	DQ22	144	CB7	167	NC
99	DQ7	122	A8	145	VSS	168	VDD
100	VSS	123	DQ23	146	DQ36	169	DQS15
101	NC	124	VSS	147	DQ37	170	DQ54
102	NC	125	A6	148	VDD	171	DQ55
103	NC	126	DQ28	149	DQS13	172	VDD
104	VDD	127	DQ29	150	DQ38	173	NC
105	DQ12	128	VDD	151	DQ39	174	DQ60
106	DQ13	129	DQS12	152	VSS	175	DQ61
107	DQS10	130	A3	153	DQ44	176	VSS
108	VDD	131	DQ30	154	RAS#	177	DQS16
109	DQ14	132	VSS	155	DQ45	178	DQ62
110	DQ15	133	DQ31	156	VDD	179	DQ63
111	NC	134	CB4	157	S0#	180	VDD
112	VDD	135	CB5	158	NC	181	SA0
113	NC	136	VDD	159	DQS14	182	SA1
114	DQ20	137	CK0	160	VSS	183	SA2
115	NC/A12	138	CK0#	161	DQ46	184	VDDSPD

NOTE:
Pin 115 is No Connect (128MB), and A12 (256MB).

Figure 2: 184-Pin DIMM Pinouts

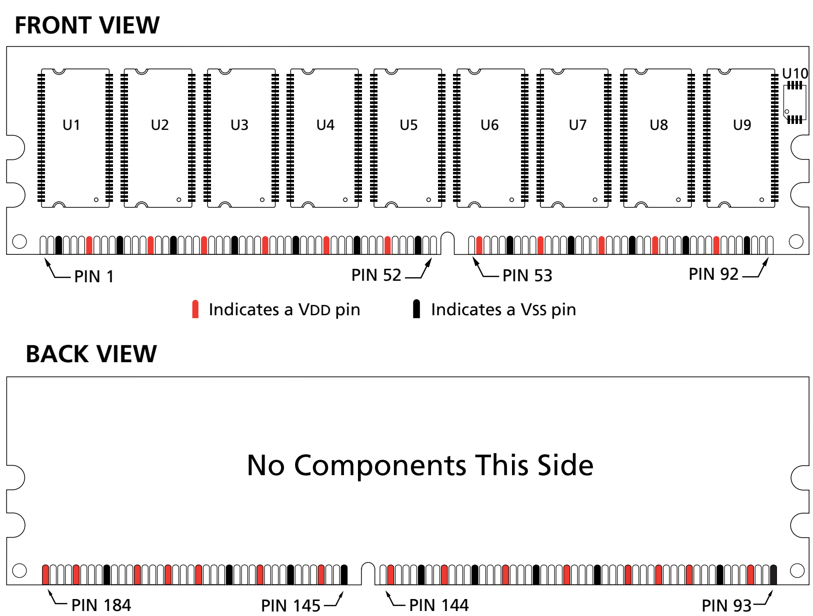


Table 5: Pin Descriptions

Refer to Pin Assignment Tables on page 3 for pin number and symbol information

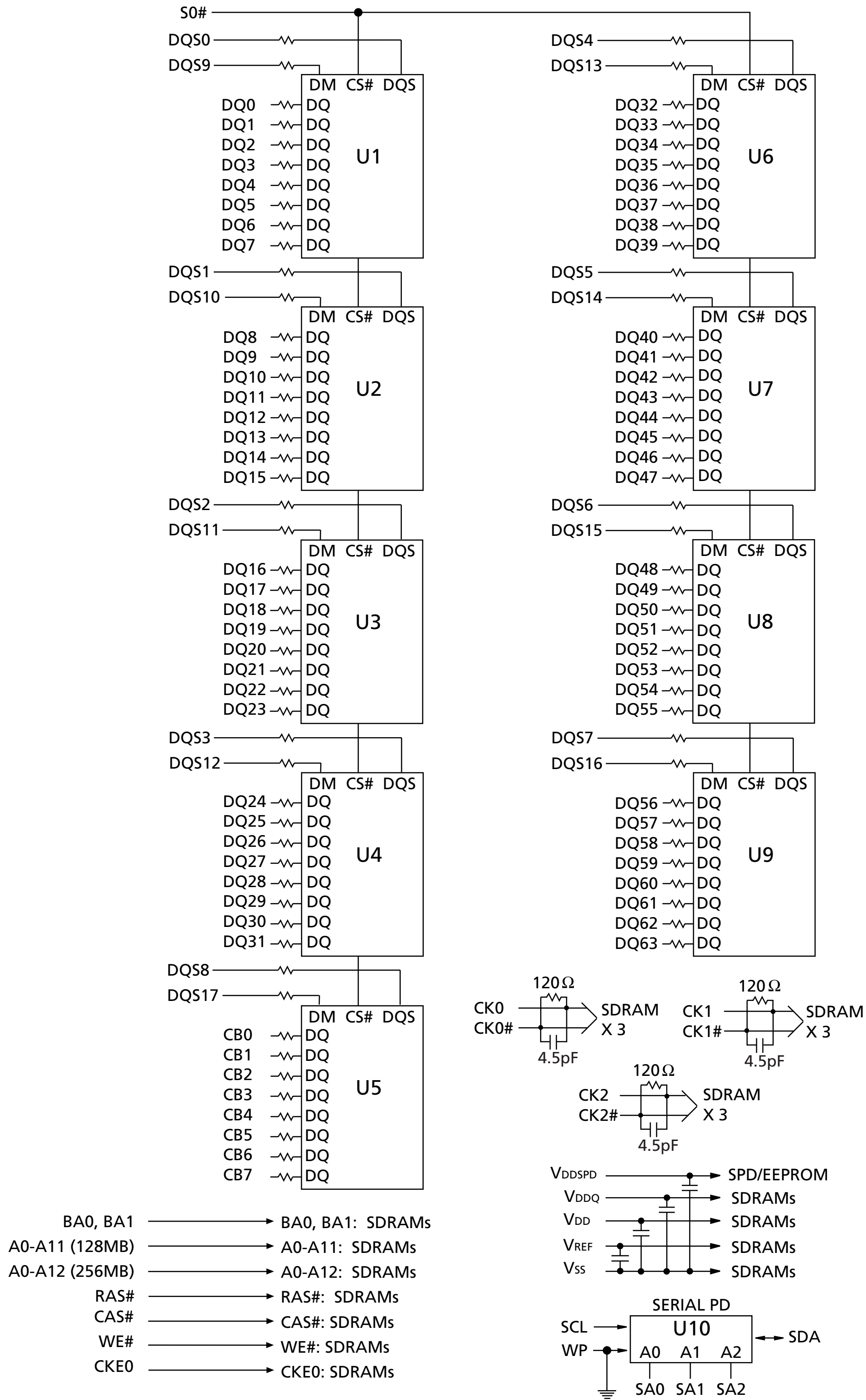
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	VREF	Input	SSTL_2 reference voltage.
63, 65, 154	WE#, CAS#, RAS#	Input	Command Inputs: WE#, RAS#, and CAS# (along with S#) define the command being entered.
16, 17, 75, 76, 137, 138	CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	Clocks: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
21	CKE0	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) internal clock signals, device input buffers, and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE0 is synchronous for all functions except for disabling outputs, which is achieved asynchronously. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWERDOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied.
157	S0#	Input	Chip Select: S# enables (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
52, 59	BA0, BA1	Input	Bank Addresses: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
27, 29, 32, 37, 41, 43, 48, 115 (256MB), 118, 122, 125, 130, 141	A0-A11 (128MB) A0-A12 (256MB)	Input	Address Inputs: Sampled during the ACTIVE command (row-address) and READ/WRITE command (column-address, with A10 defining auto precharge) to select one location out of the memory array in the respective device device bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one device bank (A10 LOW) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command.
92	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
181, 182, 183	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
91	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence- detect portion of the module.
44, 45, 49, 51, 134, 135, 142, 144	CB0-CB7	Input/Output	Data I/Os: Check bits. ECC, one-bit error detection and correction.
5, 14, 25, 36, 47, 56, 67, 78, 86, 97, 107, 119, 129, 140, 149, 159, 169, 177	DQS0-DQS17	Input/Output	Data Strobes: Output with read data, input with write data. Edge- aligned with read data, centered in write data. Used to capture write data.

Table 5: Pin Descriptions (Continued)

Refer to Pin Assignment Tables on page 3 for pin number and symbol information

2, 4, 6, 8, 12, 13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 117, 121, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162, 165, 166, 170, 171, 174, 175, 178, 179	DQ0-DQ63	Input/Output	Data I/Os: Data bus.
7, 15, 22, 30, 38, 46, 54, 62, 70, 77, 85, 96, 104, 108, 112, 120, 128, 136, 143, 148, 156, 164, 168, 172, 180	VDD	Supply	Power Supply: +2.5V +0.2V. (Please see note 50 on page 21.)
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	VSS	Supply	Ground.
184	VDDSPD	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V. This supply is isolated from the VDD/VDDQ supply.
9, 10, 71, 82, 90, 101, 102, 103, 111, 113, 115 (128MB), 158, 163, 167, 173	NC	–	No Connects.

Figure 3: Functional Block Diagram -26A, -265, -202 Speed Optimized

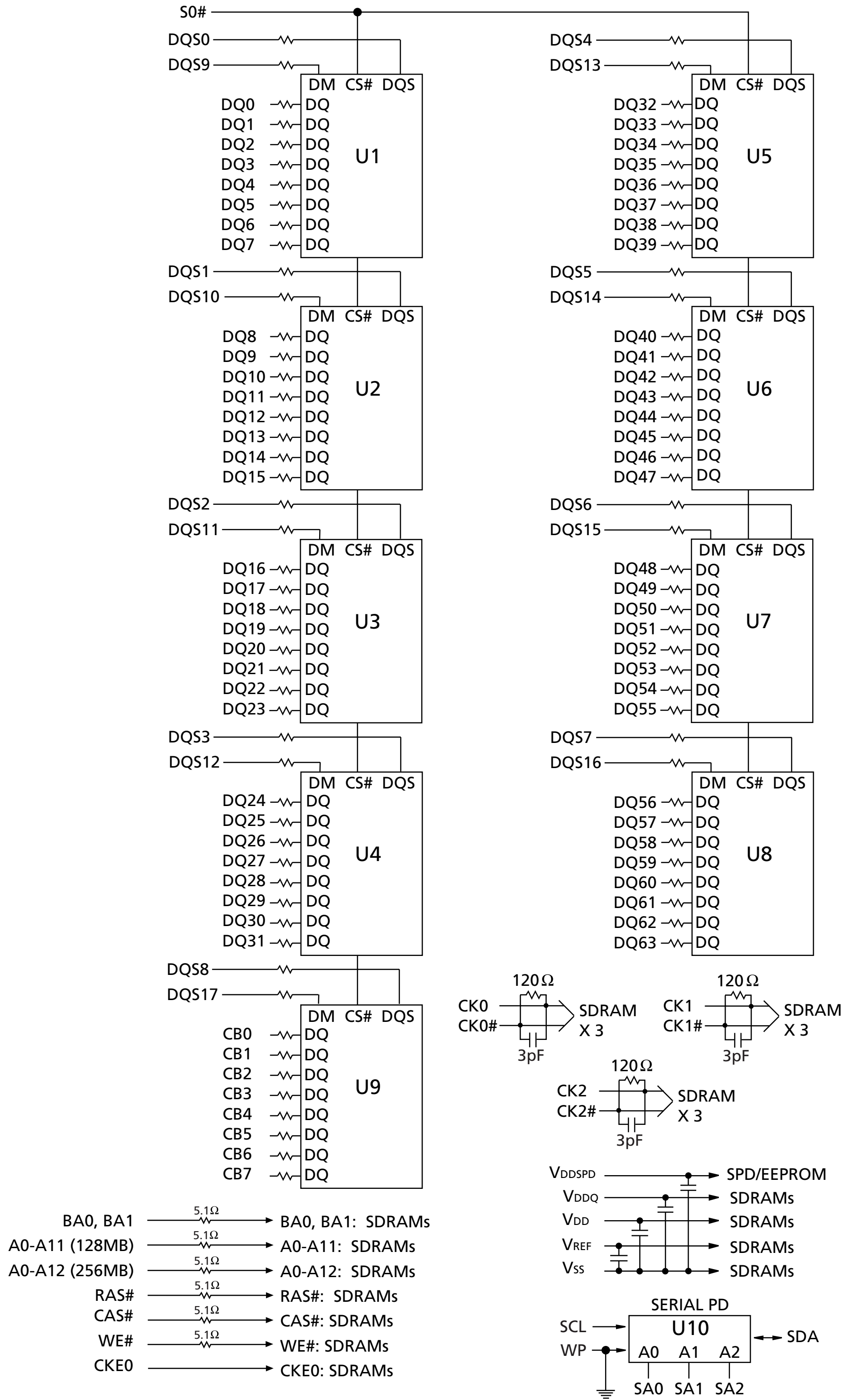


NOTE:

1. All resistor values are 22Ω unless otherwise specified.
2. Per industry standard, Micron modules utilize various component speed grades, as referenced in the module part number guide at www.micron.com/numberguide.

U1 - U9 = MT46V16M8TG DDR SDRAMs 128MB Module
U1 - U9 = MT46V32M8TG DDR SDRAMs 256MB Module

Figure 4: Functional Block Diagram -335 Speed Optimized



U1 - U9 = MT46V16M8TG DDR SDRAMs 128MB Module
U1 - U9 = MT46V32M8TG DDR SDRAMs 256MB Module

NOTE:

1. All resistor values are 22Ω unless otherwise specified.
2. Per industry standard, Micron modules utilize various component speed grades, as referenced in the module part number guide at www.micron.com/numberguide.

General Description

The MT9VDDT1672A and MT9VDDT3272A are high-speed CMOS, dynamic random-access, 128MB and 256MB memory modules organized in a x72 (ECC) configuration. These modules use internally configured quad-bank DDR SDRAM devices.

These DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

These DDR SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select device bank; A0–A11 select device row for the 128MB module, A0–A12 select device row for the 256MB module). The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

These DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAM modules, the pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 128Mb and 256Mb DDR SDRAM component data sheet.

Serial Presence-Detect Operation

These DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Mode Register Definition

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 5, Mode Register Definition Diagram, on page 9. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A11 (for the 128MB module) or A7–A12 (for the 256MB module) specify the operating mode.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 5, Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A9 when the burst length is set to two, by A2–A9 when the burst length is set to four and by A3–A9 when the burst length is set to eight (where A9 is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 6, Burst Definition Table, on page 10.

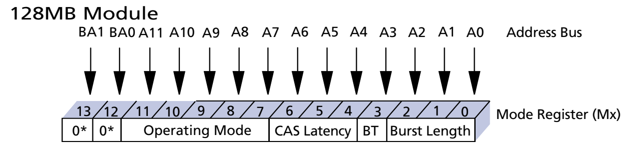
Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 2.5 clocks, as shown in Figure 6, CAS Latency Diagram, on page 10.

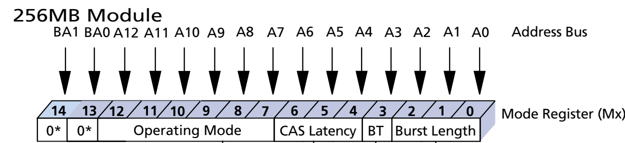
If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table 7, CAS Latency (CL) Table, on page 10, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 5: Mode Register Definition Diagram



* M13 and M12 (BA0 and BA1) must be "0, 0" to select the base mode register (vs. the extended mode register).



* M14 and M13 (BA0 and BA1) must be "0, 0" to select the base mode register (vs. the extended mode register).

M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	All other states reserved

Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7–A11 (128MB), or A7–A12 (256MB) each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9–A11 (128MB), or A7 and A9–A12 (256MB) each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7–A11, or A7–A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Table 6: Burst Definition Table

BURST LENGTH	STARTING COLUMN ADDRESS	ORDER OF ACCESSES WITHIN A BURST	
		TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTE:

1. For a burst length of two, A1–A*i* select the two-data-element block; A0 selects the first access within the block.
2. or a burst length of four, A2–A*i* select the four-data-element block; A0–A1 select the first access within the block.
3. For a burst length of eight, A3–A*i* select the eight-data-element block; A0–A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
5. *i* = 11 for 128MB module,
   i = 12 for 256MB module

Figure 6: CAS Latency Diagram

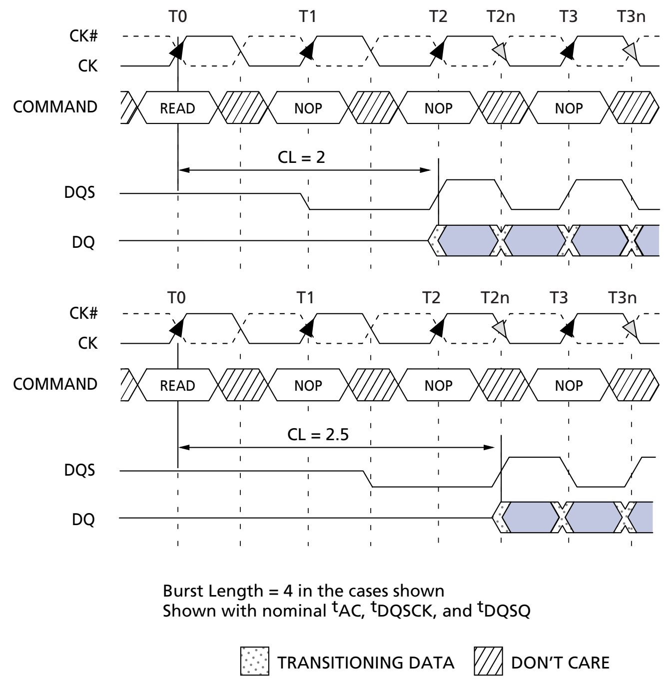


Table 7: CAS Latency (CL) Table

SPEED	ALLOWABLE OPERATING FREQUENCY (MHZ)	
	CL = 2	CL = 2.5
-335	N/A	75 ≤ f ≤ 167
-26A	75 ≤ f ≤ 133	75 ≤ f ≤ 133
-265	75 ≤ f ≤ 100	75 ≤ f ≤ 133
-202	75 ≤ f ≤ 100	75 ≤ f ≤125

Extended Mode Register

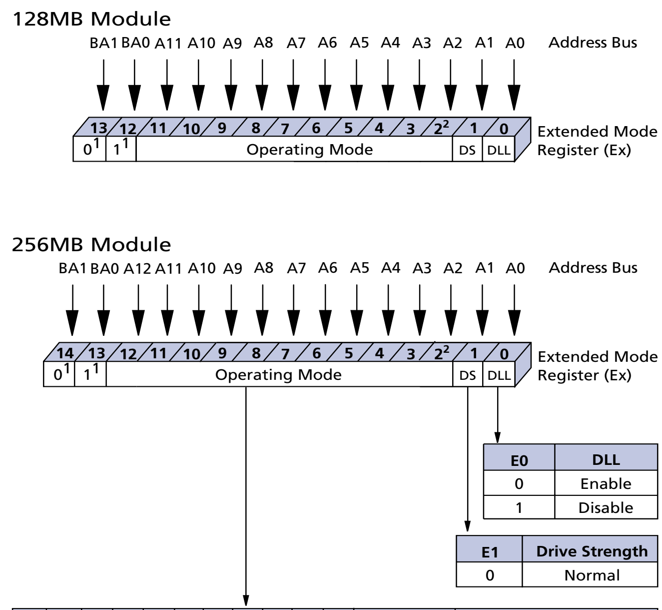
The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and output drive strength. These functions are controlled via the bits shown in Figure 7, Extended Mode Register Definition Diagram, on page 11. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both low) to reset the DLL.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Figure 7: Extended Mode Register Definition Diagram



E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2[2]	E1, E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	0	Valid	Reserved
–	–	–	–	–	–	–	–	–	–	–	–	Reserved

NOTE:

1. E13 and E12 (128MB module), or E14 and E13 (256MB Module) (BA1 and BA0) must be “0, 1” to select the Extended Mode Register (vs. the base Mode Register).
2. The QFC# option is not supported.

Commands

The Truth Tables below provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 128Mb and 256Mb DDR SDRAM component data sheets.

Table 8: Truth Table – Commands

Notes: 1

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	2
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	5
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	6
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	7, 8
LOAD MODE REGISTER	L	L	L	L	Op-Code	9

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. DESELECT and NOP are functionally interchangeable.
3. BA0–BA1 provide device bank address and A0–A11 (128MB) or A0–A12 (256MB) provide device row address.
4. BA0–BA1 provide device bank address; A0–A9 provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for read bursts with auto precharge enabled and for write bursts.
6. A10 LOW: BA0–BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0–BA1 are "Don't Care."
7. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
8. Internal refresh counter controls device row addressing; all inputs and I/Os are "Don't Care" except for CKE.
9. BA0-BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A11 (for 128MB module) or A0–A12 (for 256MB module) provide the op-code to be written to the selected mode register.

Table 9: Truth Table – DM Operation

Used to mask write data; provided coincident with the corresponding data

NAME (FUNCTION)	DM	DQS
WRITE Enable	L	Valid
WRITE Inhibit	H	X

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on VDD Supply
Relative to VSS . . . . -1V to +3.6V
Voltage on VDDQ Supply
Relative to VSSS . . . . -1V to +3.6V
Voltage on VREF and Inputs
Relative to VSS . . . . -1V to +3.6V
Voltage on I/O Pins
Relative to VSS . . . . -0.5V to VDDQ +0.5V

Operating Temperature,
T_A (ambient) . . . . .0°C to +70°C
Storage Temperature (plastic) . . . . . . -55°C to +150°C
Power Dissipation 9W
Short Circuit Output Current. 50mA

Table 10: DC Electrical Characteristics and Operating Conditions

Notes: 1–5, 14, 50; notes appear on pages 18–21; 0°C ≤ T_A ≤ +70°C

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		VDDQ	2.3	2.7	V	32, 36
I/O Supply Voltage		VDDQ	2.3	2.7	V	32, 36, 39
I/O Reference Voltage		VREF	0.49 x VDDQ	0.51 x VDDQ	V	6, 39
I/O Termination Voltage (system)		VTT	VREF - 0.04	VREF + 0.04	V	7, 39
Input High (Logic 1) Voltage		VIH(DC)	VREF + 0.15	VDD + 0.3	V	25
Input Low (Logic 0) Voltage		VIL(AC)	-0.3	VREF - 0.15	V	25
INPUT LEAKAGE CURRENT: Any input 0V ≤ VIN ≤ VDD, VREF pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE#, CKE, S#	IL	-18	18	µA	49
	CK, CK#	IL	-6	6	µA	49
	DM	IL	-2	2	µA	49
OUTPUT LEAKAGE CURRENT: (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	DQ, DQS	IOZ	-5	5	µA	49
OUTPUT LEVELS: High Current (VOUT = VDDQ - 0.373V, minimum VREF, minimum VTT)		IOH	-16.8	–	mA	33, 36
Low Current (VOUT = 0.373V, maximum VREF, maximum VTT)		IOL	16.8	–	mA	34

Table 11: AC Input Operating Conditions

Notes: 1–5, 12, 14, 50; notes appear on pages 18–21; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V +0.2V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	VIH(AC)	VREF + 0.310	–	V	25, 35
Input Low (Logic 0) Voltage	VIL(AC)	–	VREF - 0.310	V	25, 35
I/O Reference Voltage	VREF(AC)	0.49 x VDDQ	0.51 x VDDQ	V	6

Table 12: I_{DD} Specifications and Conditions (128MB)

DRAM components only
Notes: 1–5, 8, 10, 12, 50; notes appear on pages 18–21; 0°C ≤ T_A ≤ +70°C; V_{DD} = $V_{DD}Q$ = +2.5V +0.2V

PARAMETER/CONDITION		SYMBOL	MAX				UNITS	NOTES
			-335	-262	-26A/ -265	-202		
OPERATING CURRENT: One device bank; Active-Precharge; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;		I_{DD0}	TBD	TBD	945	900	mA	20, 43
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 2; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	TBD	TBD	1,080	990	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = LOW;		I_{DD2P}	TBD	TBD	27	27	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^{t}CK = ^{t}CK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM		I_{DD2F}	TBD	TBD	405	315	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = LOW		I_{DD3P}	TBD	TBD	180	180	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^{t}RC = ^{t}RAS (MAX); ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	TBD	TBD	405	315	mA	40
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); I_{OUT} = 0mA		I_{DD4R}	TBD	TBD	1,125	945	mA	20, 43, 24, 45
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	TBD	TBD	1,035	945	mA	20
AUTO REFRESH CURRENT	^{t}RC = ^{t}RFC (MIN)	I_{DD5}	TBD	TBD	1,890	1,845	mA	24, 45
	^{t}RC = 15.625µs	I_{DD5A}	TBD	TBD	45	45	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	I_{DD6}	TBD	TBD	18	18	mA	9
	Low Power	I_{DD6A}	TBD	TBD	9	9	mA	
OPERATING CURRENT: Four device bank interleaving READs (BL=4) with auto precharge, ^{t}RC =^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); Address and control inputs change only during Active, READ, or WRITE commands.		I_{DD7}	TBD	TBD	2,925	2,475	mA	20, 44

Table 13: IDD Specifications and Conditions (256MB)

DRAM components only
Notes: 1–5, 8, 10, 12, 50; notes appear on pages 18–21; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V +0.2V

PARAMETER/CONDITION		SYMBOL	MAX -335	MAX -262	MAX -26A/ -265	MAX -202	UNITS	NOTES
OPERATING CURRENT: One device bank; Active-Precharge; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;		IDD0	1,125	1,125	945	1,080	mA	20, 43
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 2; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,530	1,440	1,305	1,395	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW;		IDD2P	36	36	36	36	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; $^tCK = {}^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	450	405	405	405	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW		IDD3P	270	225	225	270	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; $^tRC = {}^tRAS$ (MAX); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	540	450	450	450	mA	42
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); IOUT = 0mA		IDD4R	1,575	1,350	1,350	1,575	mA	20, 43, 24, 45
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,395	1,215	1,215	1,710	mA	20
AUTO REFRESH CURRENT	$^tRC = {}^tRFC$ (MIN)	IDD5	2,295	2,115	2,115	2,205	mA	24, 45
	^tRC = 7.8125µs	IDD6	54	54	54	54	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	IDD7	36	36	36	36	mA	9
	Low Power	IDD7A	18	18	18	18	mA	
OPERATING CURRENT: Four device bank interleaving READs (BL=4) with auto precharge, $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); Address and control inputs change only during Active, READ, or WRITE commands.		IDD8	3,645	3,150	3,285	3,285	mA	20, 44

Table 14: Capacitance (All Modules)

Note: 11; notes appear on pages 18–21

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQs, DQSs	C_{IO}	4.0	5.0	pF
Input Capacitance: Command and Address, S0#	C_{I1}	2.0	3.0	pF
Input Capacitance: CK0, CK0# (-26A, -265, -202)	C_{I2}	12.0	15.0	pF
Input Capacitance: CK0, CK0# (-335)	C_{I2}	9	12.0	pF
Input Capacitance: CK1, CK1#, CK2, CK2# (-26A, -265, -202)	C_{I2}	10.5	13.5	pF
Input Capacitance: CKE	C_{I3}	18.0	27.0	pF

Table 15: Electrical Characteristics and Recommended AC Operating Conditions

Notes: 1–5, 8, 12–15, 29, 31, 50; notes appear on pages 18–21; 0°C ≤ T_A ≤ +70°C; V_{DD} = V_{DDQ} = +2.5V ±0.2V

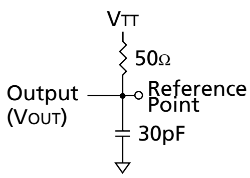
AC CHARACTERISTICS			-335		-26A/265		-202			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access window of DQ from CK/CK#		^tAC	-0.7	+0.7	-0.75	+0.75	-0.8	+0.8	ns	
CK high-level width		^tCH	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	26
CK low-level width		^tCL	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	26
Clock cycle time	CL = 2.5	^tCK (2.5)	6	13	7.5	13	8	13	ns	40, 47, 48
	CL = 2	^tCK (2)	7.5	13	7.5	13	10	13	ns	40, 47
DQ and DM input hold time relative to DQS		^tDH	0.45		0.5		0.6		ns	23, 27
DQ and DM input setup time relative to DQS		^tDS	0.45		0.5		0.6		ns	23, 27
DQ and DM input pulse width (for each input)		^tDIPW	1.75		1.75		2		ns	27
Access window of DQS from CK/CK#		^tDQSCK	-0.60	+0.60	-0.75	+0.75	-0.8	+0.8	ns	
DQS input high pulse width		^tDQSH	0.35		0.35		0.35		^tCK	
DQS input low pulse width		^tDQSL	0.35		0.35		0.35		^tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ		0.45		0.5		0.6	ns	22, 25
Write command to first DQS latching transition		^tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	^tCK	
DQS falling edge to CK rising - setup time		^tDSS	0.2		0.2		0.2		^tCK	
DQS falling edge from CK rising - hold time		^tDSH	0.2		0.2		0.2		^tCK	
Half clock period		^tHP	^tCH,^tCL		^tCH, ^tCL		^tCH, ^tCL		ns	30
Data-out high-impedance window from CK/CK#		^tHZ		+0.70		+0.75		+0.8	ns	16, 37
Data-out low-impedance window from CK/CK#		^tLZ	-0.70		-0.75		-0.8		ns	16, 38
Address and control input hold time (fast slew rate)		^tIH_F	0.75		0.90		1.1		ns	12
Address and control input setup time (fast slew rate)		^tIS_F	0.75		0.90		1.1		ns	12
Address and control input hold time (slow slew rate)		^tIH_S	0.80		1		1.1		ns	12
Address and control input setup time (slow slew rate)		^tIS_S	0.80		1		1.1		ns	12
LOAD MODE REGISTER command cycle time		^tMRD	12		15		16		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP -^tQHS		^tHP -^tQHS		^tHP- ^tQHS		ns	22, 23
Data hold skew factor		^tQHS		0.55		0.75		1	ns	

Table 15: Electrical Characteristics and Recommended AC Operating Conditions (Continued)

AC CHARACTERISTICS			-335		-26A/265		-202			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
ACTIVE to PRECHARGE command		^{t}RAS	42	70,000	40	120,000	40	120,000	ns	31
ACTIVE to READ with Auto precharge command	128MB	^{t}RAP			$^{t}RAS(MIN)$ - (burst length) * $^{t}CK/2)$				ns	40
ACTIVE to READ with Auto precharge command	256MB	^{t}RAP	18		$^{t}RAS(MIN)$ - (burst length) * $^{t}CK/2)$				ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^{t}RC	60		65		70		ns	
AUTO REFRESH command period		^{t}RFC	72		75		80		ns	45
ACTIVE to READ or WRITE delay		^{t}RCD	18		20		20		ns	
PRECHARGE command period		^{t}RP	18		20		20		ns	
DQS read preamble		$^{t}RPRE$	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CK	37
DQS read postamble		$^{t}RPST$	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	12		15		15		ns	
DQS write preamble		$^{t}WPRE$	0.25		0.25		0.25		^{t}CK	
DQS write preamble setup time		$^{t}WPRES$	0		0		0		ns	18, 19
DQS write postamble		$^{t}WPST$	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	17
Write recovery time		^{t}WR	15		15		15		ns	
Internal WRITE to READ command delay		^{t}WTR	1		1		1		^{t}CK	
Data valid output window		na	^{t}QH - $^{t}DQSQ$		^{t}QH - $^{t}DQSQ$		^{t}QH - $^{t}DQSQ$		ns	22
REFRESH to REFRESH command interval	128MB	$^{t}REFC$		140.6		140.6		140.6	µs	21
REFRESH to REFRESH command interval	256MB	$^{t}REFC$		70.3		140.6		140.6	µs	21
Average periodic refresh interval	128MB	$^{t}REFI$		15.6		15.6		15.6	µs	21
Average periodic refresh interval	256MB	$^{t}REFI$		7.8		7.8			µs	21
Terminating voltage delay to V_{DD}		^{t}VTD	0		0				ns	
Exit SELF REFRESH to non-READ command		$^{t}XSNR$	75		75				ns	
Exit SELF REFRESH to READ command		$^{t}XSRD$	200		200				^{t}CK	

Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:

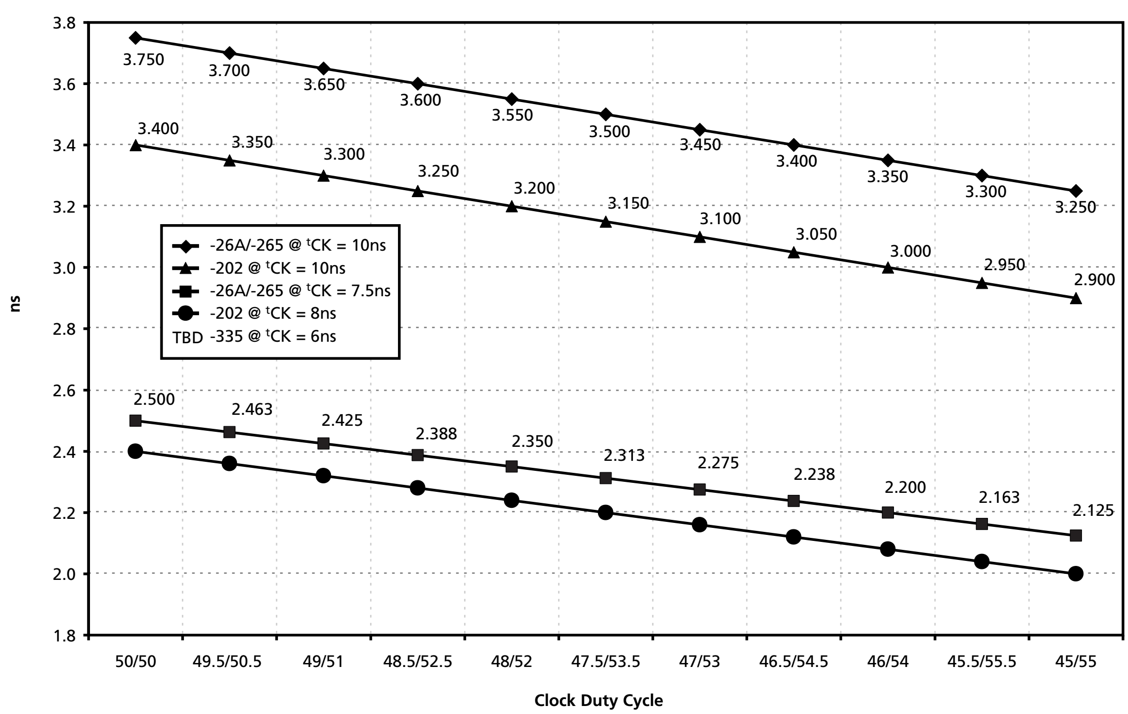


4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal $V_{DD}Q/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from $V_{DD}Q/2$, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} by-pass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2 for -262, -26A, and -202, CL = 2.5 for -265 and -335 with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{DD} = +2.5V ±0.2V, $V_{DD}Q$ = +2.5V ±0.2V, V_{REF} = V_{SS}, f = 100 MHz, T_A = 25°C, V_{OUT} (DC) = $V_{DD}Q/2$, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. Command/Address input slew rate = 0.5V/ns. For -335 and -262, -26A, and -265 with slew rates 1V/ns and faster, ^{t}IS and ^{t}IH are reduced to 900ps. If the slew rate is less than 0.5V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. ^{t}IH has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x $V_{DD}Q$ is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
16. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
20. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. tRAS (MAX) for Idd measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
21. The refresh period 64ms. This equates to an average refresh rate of 15.625µs (128MB module) 7.8125µs (256MB module). However, an AUTO REFRESH command must be asserted at least

once every 140.6µs (128MB module) or 70.3µs (256MB module); burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.

22. The valid data window is derived by achieving other specifications - ^{t}HP (^{t}CK/2), tDQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. Figure 8, Derating Data Valid Window (^{t}QH - ^{t}DQSQ), shows the derating curves for duty cycles ranging between 50/50 and 45/55.
23. Each byte lane has a separate DQS, with DQ0–DQ7.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a) Sustain a constant slew rate from the current AC level through to the target AC level, V_{IL}(AC) or V_{IH}(AC).
    b) Reach at least the target AC level.
    c) After the AC target level is reached, continue to maintain at least the target DC level, V_{IL}(DC) or V_{IH}(DC).
26. CK and CK# input slew rate must be ≥ 1V/ns (≥ 2V/ns if measured differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.
28. V_{DD} must not vary more than 4 percent if CKE is not active while any device bank is active.
29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
30. ^{t}HP (MIN) is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs, collectively during bank active.

Figure 8: Derating Data Valid Window
(^{t}QH - ^{t}DQSQ)



31. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS (MIN) can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch must be less than 1/3 of the clock cycle and not more than +400mV or 2.9V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V, whichever is more positive. The DC average cannot go below 2.3V minimum.
33. Normal Output Drive Curves:
    a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 9, Pull-Down Characteristics.
    b) The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 9, Pull-Down Characteristics.
    c) The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 10, Pull-Up Characteristics.
    d) The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 10, Pull-Up Characteristics.
    e) The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
    f) The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent, for device drain-to-source voltages from 0.1V to 1.0V.
34. The voltage levels used are derived from a minimum VDD level and the refernced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
35. VIH overshoot: VIH (MAX) = VDDQ+1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL (MIN) = -1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
36. VDD and VDDQ must track each other.
37. This maximum value is derived from the referenced test load. In practice, the values obtained in a typical terminated design may reflect up to 310ps less for ^{t}HZ (MAX) and the last DVW. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition. ^{t}LZ (MIN) will prevail over ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
38. For slew rates of greater than 1V/ns the (LZ) transition will start about 310ps earlier.
39. During initialzation, VDDQ, VTT, and VREF must be equal to or less than VDD + 0.3V. Alternatively, VTT may be 1.35V maximum during power up, even if VDD/VDDQ are 0.0V, provided a minimum of 42 ohms of series resistance is used between the VTT supply and the input pin.

Figure 9: Pull-Down Characteristics

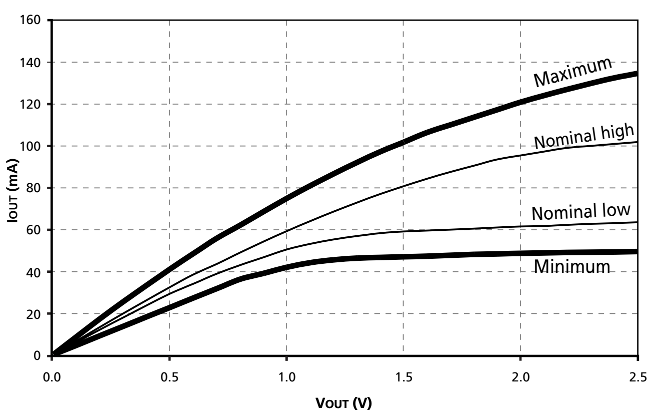
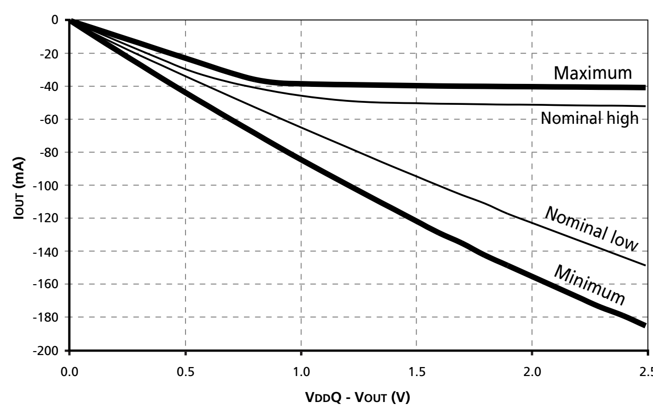


Figure 10: Pull-Up Characteristics



40. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. $^tRAP \geq {^tRCD}$.
42. For -335, -262, -26A, and -265 speed grades, IDD3N is specified to be 35mA x (# of DDR SDRAM devices) at 100 MHz.
43. Random addressing changing and 50 percent of data changing at every transfer.
44. Random addressing changing and 100 percent of data changing at every transfer.
45. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
46. IDD2N specifies the DQ, DQS and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is "worst case."
47. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.
48. Min ^{t}CK value at CL=2.5 in the SPD for and -26A speeds is 0.7ns, to facilitate proper system operation.
49. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
50. The -335 module speed grade, using the -6R speed device, has VDD (MIN) = 2.4V.

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 11, Data Validity, and Figure 12, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 12, Definition of Start and Stop).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 11: Data Validity

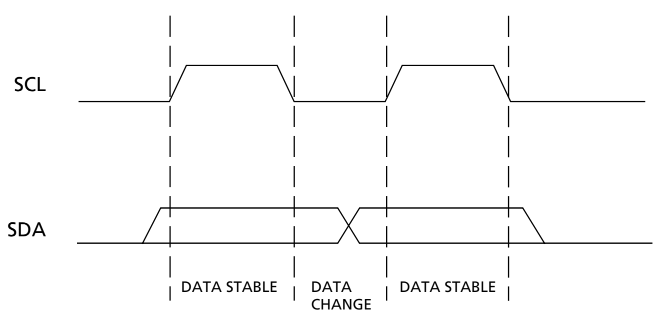


Figure 12: Definition of Start and Stop

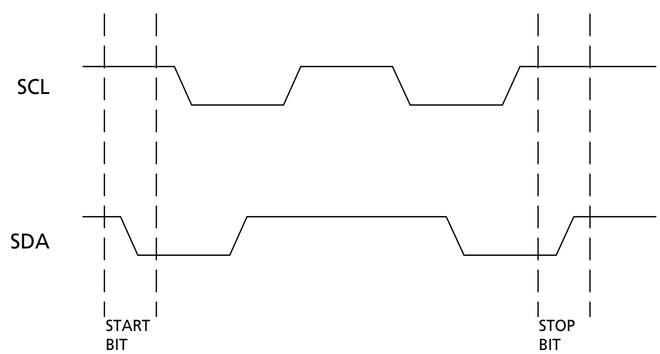


Figure 13: Acknowledge Response from Receiver

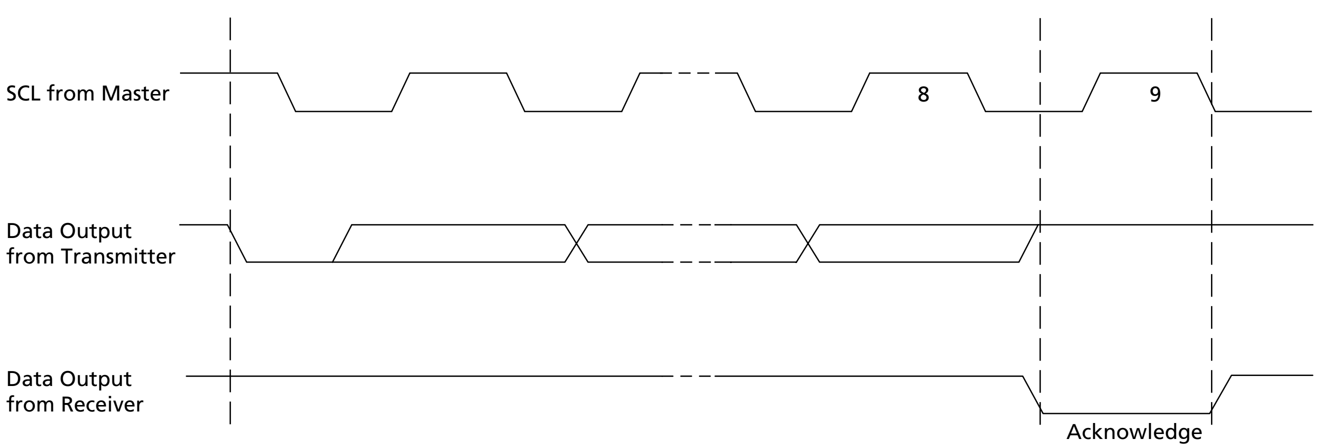


Table 16: EEPROM Device Select Code

Most significant bit (b7) is sent first

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			$R\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	$R\overline{W}$
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	$R\overline{W}$

Table 17: EEPROM Operating Modes

MODE	$R\overline{W}$ BIT	$\overline{WC}$	BYTES	INITIAL SEQUENCE
Current Address Read	1	V_{IH} or V_{IL}	1	START, Device Select, $R\overline{W}$ = ‘1’
Random Address Read	0	V_{IH} or V_{IL}	1	START, Device Select, $R\overline{W}$ = ‘0’, Address
	1	V_{IH} or V_{IL}	1	reSTART, Device Select, $R\overline{W}$ = ‘1’
Sequential Read	1	V_{IH} or V_{IL}	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, $R\overline{W}$ = ‘0’
Page Write	0	V_{IL}	≤ 16	START, Device Select, $R\overline{W}$ = ‘0’

Figure 14: SPD EEPROM Timing Diagram

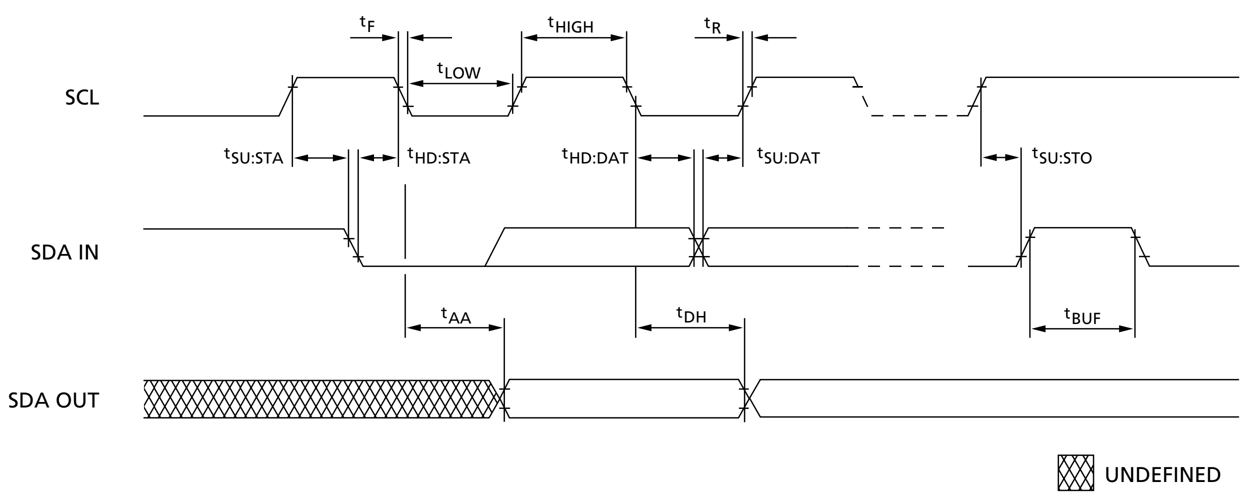


Table 18: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DD}	3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: IOUT = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: VIN = GND to VDD	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: VOUT = GND to VDD	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = VDD - 0.3V; All other inputs = V_{SS} or V_{REF}	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA

Table 19: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^tAA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^tBUF	4.7		µs	
Data-out hold time	^tDH	300		ns	
SDA and SCL fall time	^tF		300	ns	
Data-in hold time	$^tHD{:}DAT$	0		µs	
Start condition hold time	$^tHD{:}STA$	4		µs	
Clock HIGH period	^tHIGH	4		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		100	ns	
Clock LOW period	^tLOW	4.7		µs	
SDA and SCL rise time	^tR		1	µs	
SCL clock frequency	^tSCL		100	KHz	
Data-in setup time	$^tSU{:}DAT$	250		ns	
Start condition setup time	$^tSU{:}STA$	4.7		µs	
Stop condition setup time	$^tSU{:}STO$	4.7		µs	
WRITE cycle time	^tWRC		10	ms	1

NOTE:

1. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 20: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; notes at end of SPD Matrix

BYTE	DESCRIPTION	ENTRY (VERSION)	MT9VDDT1672A	MT9VDDT3272A
0	Number of Bytes Used by Micron	128	80	80
1	Total Number of SPD Memory Bytes	256	08	08
2	Memory Type	SDRAM DDR	07	07
3	Number of Row Addresses	12 or 13	0C	0D
4	Number of Column Addresses	10	0A	0A
5	Number of Ranks	1	01	01
6	Module Data Width	72	48	48
7	Module Data Width (Continued)	0	00	00
8	Module Voltage Interface Levels	SSTL 2.5V	04	04
9	SDRAM Cycle Time, ^{t}CK, (CAS Latency = 2.5) (See note 1)	6ns (-335) 7ns (-262/-26A) 7.5ns (-265) 8ns (-202)	60 70 75 80	60 70 75 80
10	SDRAM Access From Clock, ^{t}AC (CAS Latency = 2.5)	0.7ns (-335) 0.75ns (-262/-265/-26A) 0.8ns (-202)	70 75 80	70 75 80
11	Module Configuration Type	ECC	02	02
12	Refresh Rate/Type	15.6 or 7.81µs/SELF	80	82
13	SDRAM Width (Primary SDRAM)	8	08	08
14	Error-Checking SDRAM Data Width	8	08	08
15	Minimum Clock Delay, Back -to- Back	1	01	01
	Random Column Access			
16	Burst Lengths Supported	2, 4, 8	0E	0E
17	Number of Banks on SDRAM Device	4	04	04
18	CAS Latencies Supported	2, 2.5	0C	0C
19	CS Latency	0	01	01
20	WE Latency	1	02	02
21	SDRAM Module Attributes	Unbuffered, Diff CLK	20	20
22	SDRAM Device Attributes: General	Fast/concurrent auto precharge	00/C0 (See note 2)	C0
23	SDRAM Cycle Time, ^{t}CK (CAS Latency = 2)	7.5ns (-335/-262/-26A) 10ns (-202/-265)	75 A0	75 A0
24	SDRAM Cycle Time, ^{t}CK (CAS Latency = 2) (See note 1)	0.7ns (-335) 0.75ns (-262/-265/-26A) 0.8ns (-202)	70 75 80	70 75 80
25	SDRAM Cycle Time, ^{t}CK (CAS Latency = 1)	–	00	00
26	SDRAM Access From CK , (CAS latency = 1)	–	00	00
27	Minimum Row Precharge Time, ^{t}RP	18ns (-335) 20ns (-262) 20ns (-202/-265/-26A)	48 3C 50	48 3C 50
28	Minimum Row Active To Row Active, ^{t}RRD	12ns (-335) 15ns (-202/-265/-26A)/-262	30 3C	30 3C
29	Minimum RAS# to CAS# Delay, ^{t}RCD	18ns (-335) 20ns (-262) 20ns (-202/-265/-26A)	48 3C 50	48 3C 50

Table 20: Serial Presence-Detect Matrix (Continued)

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; notes at end of SPD Matrix

BYTE	DESCRIPTION	ENTRY (VERSION)	MT9VDDT1672A	MT9VDDT3272A
30	Minimum RAS# Pulse Width, ^{t}RAS	42ns (-335) 45ns (-262/-265/-26A) 40ns (-202)	2A 2D 28	2A 2D 28
31	Module Rank Density	128MB or 256MB	20	40
32	Address and Command Setup Time, ^{t}IS (See note 3)	0.8ns (-335) 1.0ns (-262/-265/-26A) 1.1ns (-202)	80 A0 B0	80 A0 B0
33	Address and Command Hold Time, ^{t}IH (See note 3)	0.8ns (-335) 1.0ns (-262/-265/-26A) 1.1ns (-202)	80 A0 B0	80 A0 B0
34	Data/Data Mask Input Setup Time, ^{t}DS	0.45ns (-335 0.5ns (-262/-265/-26A) 0.6ns (-202)	45 50 60	45 50 60
35	Data/Data Mask Input Hold Time, ^{t}DH	0.45ns (-335 0.5ns (-262/-265/-26A) 0.6ns (-202)	45 50 60	45 50 60
36-40	Reserved		00	00
41	Minimum Active/Auto Refresh Time, (^{t}RC)	60ns (-335/-262) 65ns (-265/-26A) 70ns (-202)	3C 41 46	3C 41 46
42	Minimum Auto Refresh to Active/ Auto Refresh Command Period, (^{t}RFC)	72ns (-335) 75ns (-262/-265/-26A) 80ns (-202)	48 4B 50	48 4B 50
43	Maximum Cycle Time, (^{t}CK (MAX))	12ns (-335) 13ns (-202/-265/-26A/-262)	30 34	30 34
44	Maximum DQS-DQ Skew Time, (^{t}DQSQ)	0.45ns (-335) 0.5ns (-262-265/-26A) 0.6ns (-202)	2D 32 3C	2D 32 3C
45	Maximum Read Data Hold Skew Factor, (^{t}QHS)	0.6ns (-335) 0.75ns (-262/-265/-26A) 1ns (-202)	60 75 A0	60 75 A0
46-61	Reserved		00	00
62	SPD Revision	Release 0.0	00	00
63	Checksum for Bytes 0–62	-335 -262 -26A -265 -202	*na*/10 (See note 2) 94 05/C5 (See note 2) 35/F5 (See note 2) D0/90 (See note 2)	33 B7 E8 18 B3
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C
65-71	Manufacturer's JEDEC ID Code (Continued)		00	00
72	Manufacturing Location	01–11	01–0B	01–0B
73-90	Module Part Number (ASCII)		Variable Data	Variable Data
91	PCB Identification Code	1–9	01–09	01–09
92	Identification Code (Continued)	0	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data

Table 20: Serial Presence-Detect Matrix (Continued)

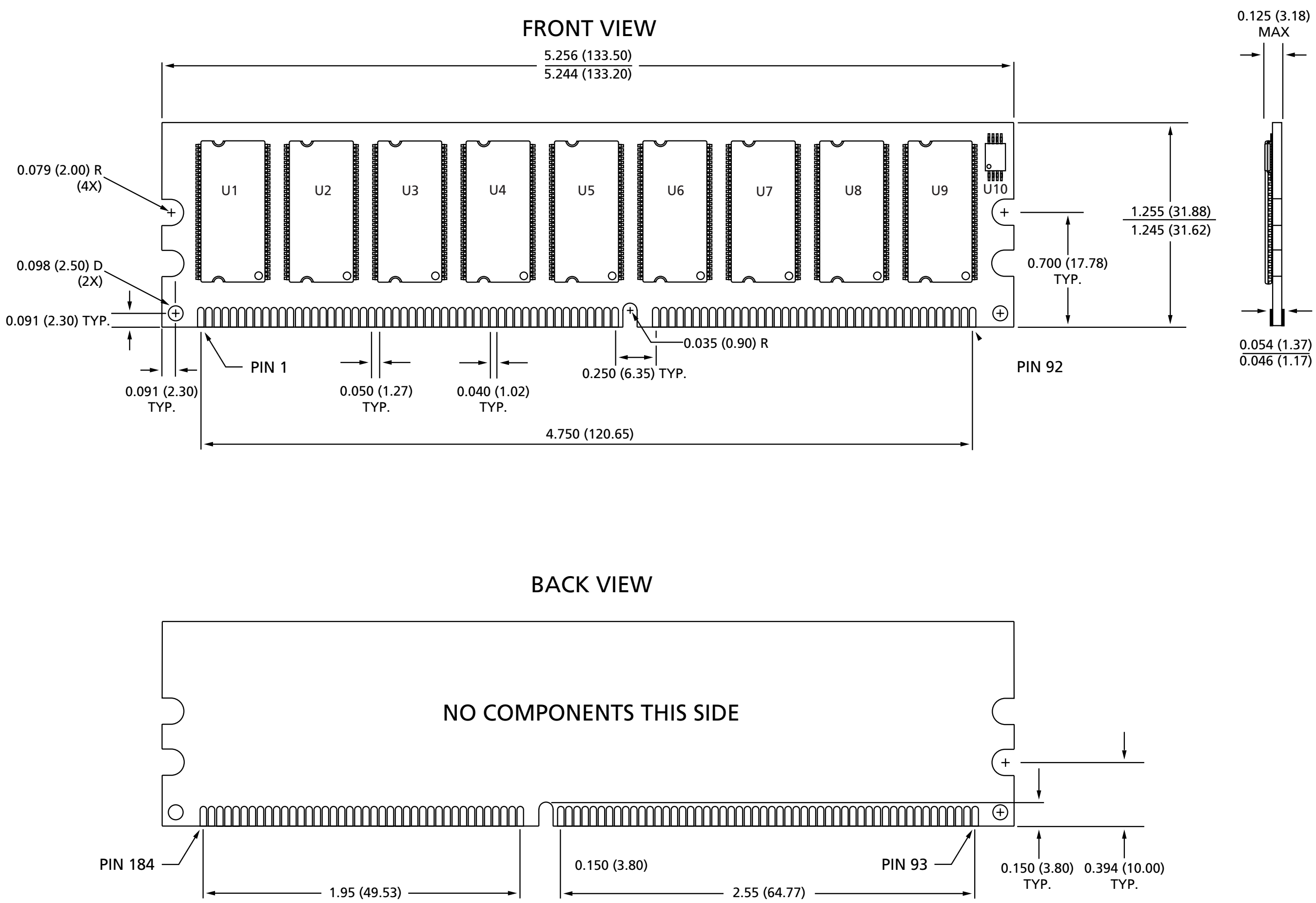
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; notes at end of SPD Matrix

BYTE	DESCRIPTION	ENTRY (VERSION)	MT9VDDT1672A	MT9VDDT3272A
94	Week of Manufacture in BCD		Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data
99-127	Manufacturer-Specific Data (RSVD)		–	–

NOTE:

1. The value of ^{t}CK for -26A modules is set at 7.0ns. Component spec. value is 7.5ns.
2. Supports Fast/Concurrent Auto Precharge. Values are listed in the form "without Concurrent Auto Precharge" / "with Concurrent Auto Precharge." Contact Factory for additonal information regarding this option.
3. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.

Figure 15: 184-Pin DIMM Dimensions



NOTE:

All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Data Sheet Designation

Released (No Mark): This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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Revision History

Rev. B, Released, 2/03 .... 2/03

- Added Low Power option
- Updated Idd, Capacitance, DC Electrical values
- Updated format
- Added -335 and -262 speed grades
- Added Pf-free option

Rev. A, Released, 01/02 .... 01/02

- New data sheet