

Version : 1.4

TECHNICAL SPECIFICATION

MODEL NO. : PW084XS1

Customer's Confirmation

Customer _____

Date _____

By _____

PVI's Confirmation

Confirmed By _____

Prepared By _____

FOR MORE INFORMATION:
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1. Application

This technical specification applies to 8.4" color TFT-LCD module, PW084XS1. The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system.

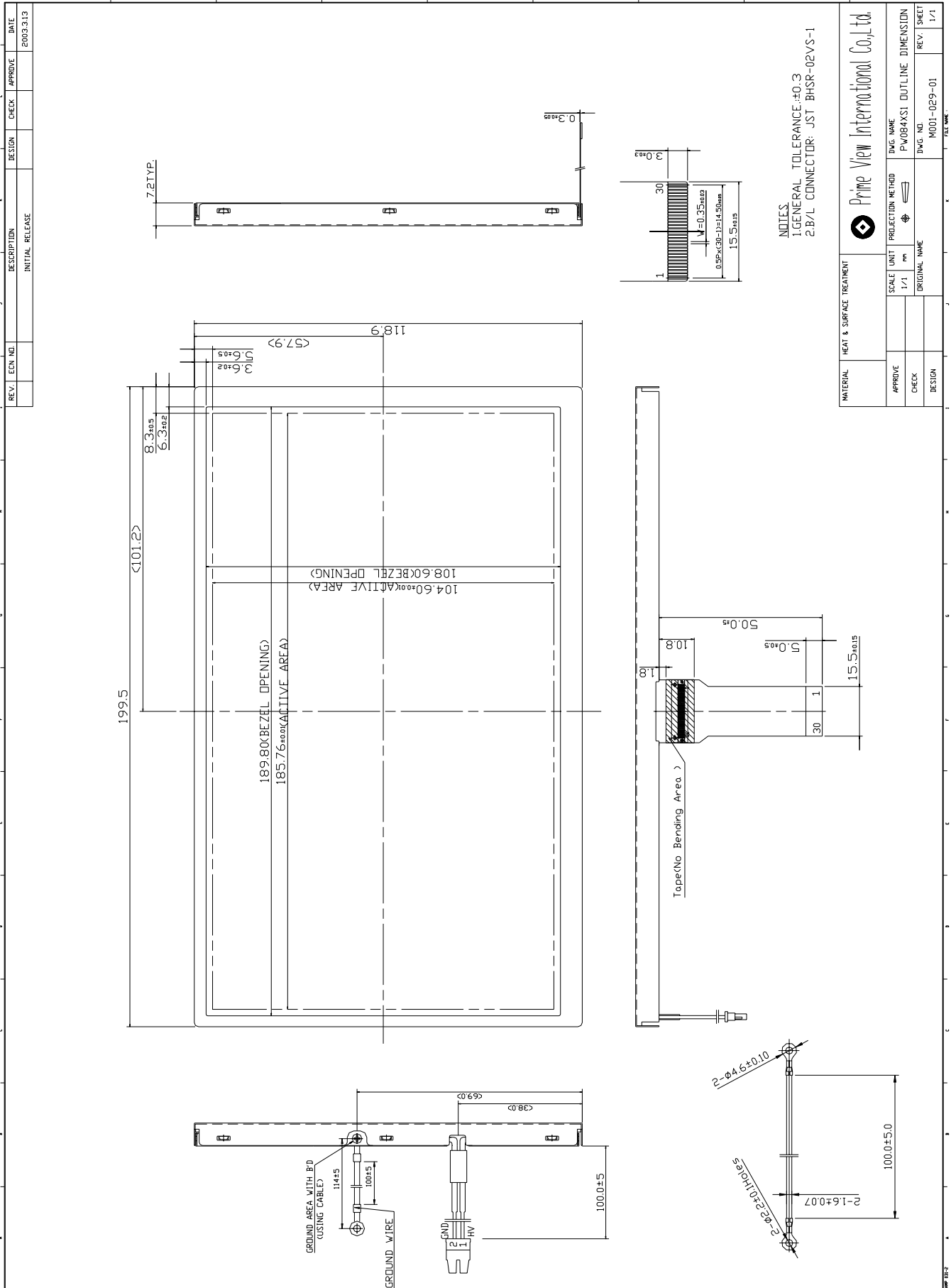
2. Features

- . Pixel in stripe configuration
- . Slim and compact
- . High Brightness
- . Image Reversion : Up/Down and Left/Right
- . Wide Viewing Angle
- . Support multi display mode
(If you use this mode, you must use PVI-1004C's timing controller (mode by PVI))

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	8.4 (16:9 diagonal)	Inch
Display Format	1440 (H) x234(V)	dot
Active Area	185.76 (H)x104.60 (V)	mm
Dot Pitch	0.129(H)x0.447(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	199.5(W)x 118.9(H)x 7.4(D)(typ.)	mm
Surface Treatment	Anti-Glare+WV film	
Weight	258±5	g

4. Mechanical Drawing of TFT-LCD Module



NOTES:
 1. GENERAL TOLERANCE: ±0.3
 2. B/L CONNECTOR: JST BHSR-02VS-1

MATERIAL	HEAT & SURFACE TREATMENT	Prime View International Co., Ltd.	
APPROVE	SCALE UNIT	PROJECTION METHOD	DWG. NAME
CHECK	1/1	1st	PW084XS1 OUTLINE DIMENSION
DESIGN	DESIGN NAME	DESIGN NO.	REV. SHEET
		M001-029-01	1/1
			FILE NAME

5. Input / Output Terminals

LCD Module Connector

FPC Down Connect , 30 Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	V _{CC}	I	Supply voltage of logic control circuit for gate driver	Note 5-3
3	NC	-	No connection	
4	V _{EE}	I	Negative power gate driver	Note 5-4
5	NC	-	No connection	
6	V _{GH}	I	Positive power for gate driver	Note 5-5
7	NC	-	No connection	
8	STVD	I/O	Vertical start pulse	Note 5-1
9	STVU	I/O	Vertical start pulse	
10	CKV	I	Shift clock for gate driver	
11	U/D	I	Up / Down Control for gate driver	Note 5-1
12	OE3	I	Output enable for gate driver	
13	OE2	I	Output enable for gate driver	
14	OE1	I	Output enable for gate driver	
15	V _{COM}	I	Common electrode voltage	
16	STHL	I/O	Start pulse for source driver	Note 5-2
17	V _{SS2}	-	Ground for analog circuit	
18	V _R	I	Video Input R	
19	V _G	I	Video Input G	
20	V _B	I	Video Input B	
21	V _{SS1}	-	Ground for digital circuit	
22	V _{DD2}	I	Supply power for analog circuit	Note 5-6
23	CPH1	I	Sampling and shift clock for source driver	
24	CPH2	I	Sampling and shift clock for source driver	
25	CPH3	I	Sampling and shift clock for source driver	
26	V _{DD1}	I	Supply power for digital circuit	Note 5-7
27	R/L	I	Left / Right Control for source driver	Note 5-2
28	NC	I	No Connection	
29	OEH	I	Output enable for source driver	
30	STHR	I/O	Start pulse for source driver	Note 5-2

Note 5-1

U/D	STVD	STVU	scanning direction
V _{CC}	Input	output	down to up
GND	Output	input	up to down

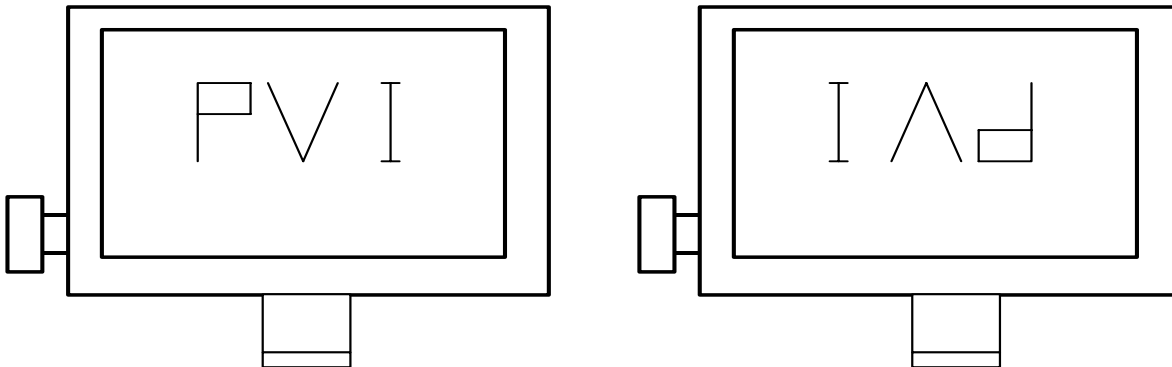
Note 5-2

R/L	STHL	STHR	scanning direction
V _{CC}	output	input	left to right
GND	input	output	right to left

The definitions of Note 5-1,5-2

U/D(PIN 11)=Low R/L(PIN 27)=High

U/D(PIN 11)=High R/L(PIN 27)=Low



Note 5-3 : V_{CC} TYP. = +5V

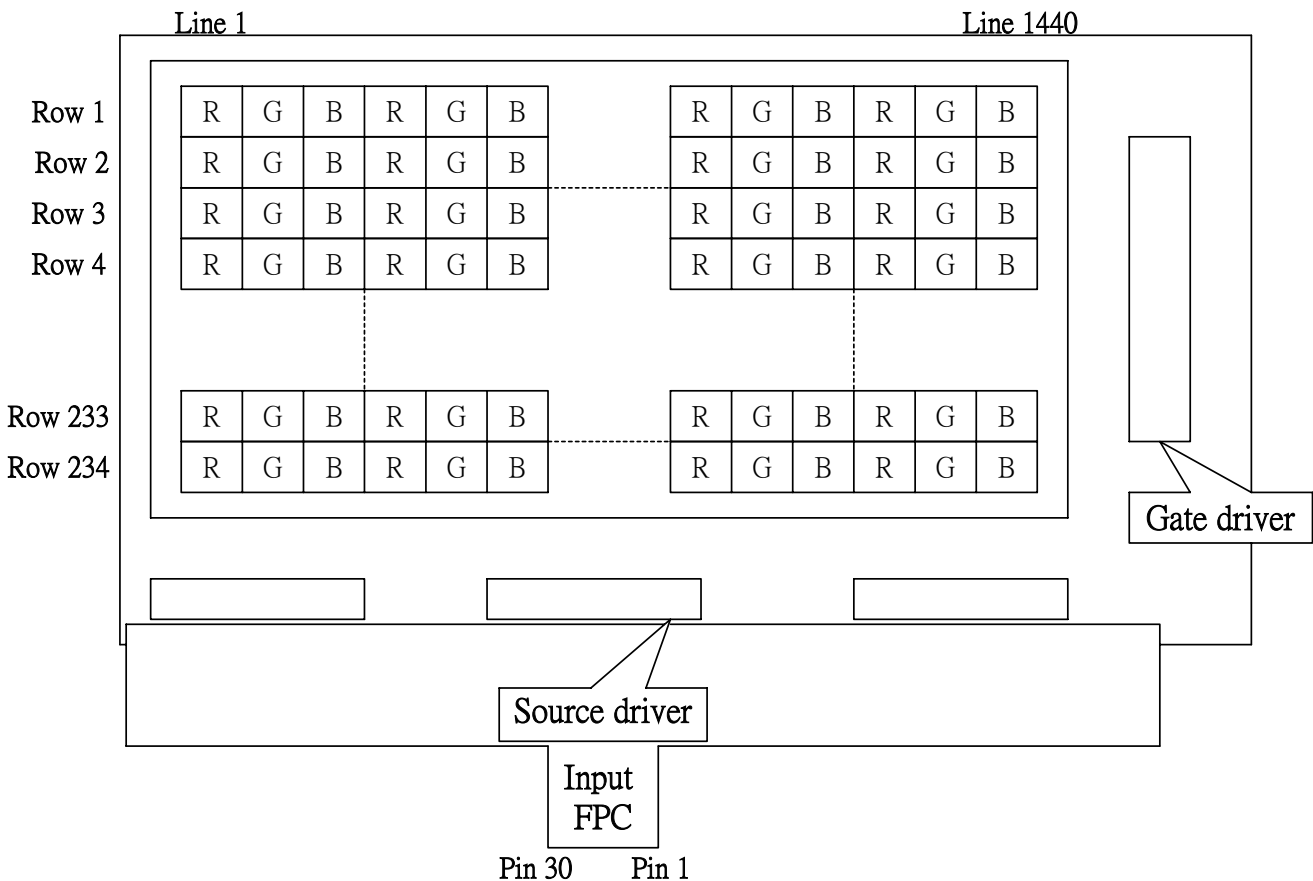
Note 5-4 : V_{EE} TYP. = -12V

Note 5-5 : V_{GH} TYP. = +17V

Note 5-6 : V_{DD2} TYP. = +5V

Note 5-7 : V_{DD1} TYP. = +5V

6. Pixel Arrangement and input connector pin NO.



7. Absolute Maximum Ratings

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver	V_{DD2}	-0.3	+5.8	V	
	V_{DD1}	-0.3	+7.0	V	
Supply Voltage For Gate Driver	V_{CC}	-0.3	+6.0	V	
	$V_{GH}-V_{EE}$	-0.3	+40.0	V	
	H Level V_{GH}	-0.3	+25.0	V	
	L Level V_{EE}	-16	+0.3	V	
Analog Signal Input Level	V_R, V_G, V_B	-0.2	$V_{DD1}+0.2$	V	Note 7-1
Storage Temperature		-30	+80	°C	
Operation Temperature		-20	+80	°C	Note 7-2

Notes 7-1 : Analog Input Voltage means V_R, V_G, V_B .

Notes 7-2 : Optical characteristics shown in Table 10-1 are measured under $T_a=+25^{\circ}\text{C}$.

8. Electrical Characteristics
8-1) Recommended Driving condition for TFT-LCD panel

Parameter	Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply Voltage For Source Driver	Analog V_{DD2}	+4.5	+5.0	+5.5	V	
	Logic V_{DD1}	+4.5	+5.0	+5.5	V	
Supply Voltage For Gate Driver	H level V_{GH}	+15	+17	+19	V	
	L level $V_{EE\ DC}$	-13.0	-12	-10.5	V	DC Component of V_{EE}
	$V_{EE\ AC}$		+6.0		V_{P-P}	AC Component of V_{EE}
	Logic V_{CC}	+4.5	+5.0	+5.5	V	
Analog Signal input Level	Amplitud	+0.3		$V_{CC}-0.3$	V	
Digital input voltage	H level V_{IH}	$0.7 V_{DD1}$	-	V_{DD1}	V	
	L level V_{IL}	-0.3	-	$0.3 V_{DD1}$	V	
Digital output voltage	H level V_{OH}	$0.7 V_{DD1}$	-	V_{DD1}	V	
	L level V_{OL}	-0.3	-	$0.3 V_{DD1}$	V	
V_{COM}	$V_{COM\ AC}$	-	+6.0	-	V_{P-P}	AC Component of V_{COM}
	$V_{COM\ DC}$	1.6	1.8	2.0	V	DC Component of V_{COM} Note 8-1

Note 8-1 : PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is $1.8V\pm 1V$, every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

8-2) Back Light driving (JST BHSR-02VS-1 ,Pin No. : 2)

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	Wire color: pink
2	VL2	Input terminal (Low voltage side)	Wire color: white Note 8-2

Note 8-2 : Low voltage side of back light inverter connects with Ground of inverter circuits.

Recommended driving condition for back light

Ta= 25 °C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V _L	585	637	716	Vrms	
Lamp current	I _L	4	6	8	mA	Note 8-3
Lamp frequency	P _L	40	55	80	KHz	Note 8-4
Starting voltage(25°C) (Reference Value)	V _s			930	Vrms	Note 8-5
Starting voltage(0°C) (Reference Value)	V _s			1170	Vrms	Note 8-5

Note 8-3 : In order to satisfy the quality of B/L , no matter use what kind of inverter , the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-4 : The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.

Note 8-5 : This value is not output voltage of inverter.
The voltage of inverter must larger than the starting voltage.
The kick-off time must larger than 1 second.

8-3) Power Consumption

Ta= 25 °C

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I _{GH}	V _{GH} = +17V	0.11	0.17	mA	
Supply current for Gate Driver (Low level)	I _{EE}	V _{EE} = -12V	1.12	1.68	mA	
Supply current for Source Driver(Digital)	I _{DD1}	V _{DD1} = +5V	1.80	4.50	mA	
Supply current for Source Driver(Analog)	I _{DD2}	V _{DD2} = +5V	10.5	15.0	mA	
Supply current for Gate Driver (Digital)	I _{CC}	V _{CC} = +5V	0.02	0.05	mA	
LCD Panel Power Consumption			76.9	120.8	mW	Note 8-6
Back Light Lamp Power Consumption			3.82		W	Note 8-7

Note 8-6 : The power consumption for back light is not included.

Note 8-7 : Back light lamp power consumption is calculated by I_L×V_L.

8-4) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
Rising time	t_r	-	-	10	ns	
Falling time	t_f	-	-	10	ns	
High and low level pulse width	t_{CPH}	9.2	9.6	10.0	MHz	CPH1~CPH3
CPH pulse duty	t_{CWH}	30	50	70	%	CPH1~CPH3
STH setup time	t_{SUH}	20	-	-	ns	STHR,STHL
STH hold time	t_{HDH}	20	-	-	ns	STHR,STHL
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STHR,STHL
STH period	t_H	61.5	63.5	65.5	μs	STHR,STHL
OEH pulse width	t_{OEH}	-	1.40	-	μs	OEH
Sample and hold disable time	t_{DIS1}	-	7.43	-	μs	
OEV pulse width	t_{OEV}	-	18	-	μs	OEV
CKV pulse width	t_{CKV}	-	31.75	-	μs	CKV
Clean enable time	t_{DIS2}	-	9.0	-	μs	
Horizontal display start	t_{SH}	-	0	-	$t_{CPH}/3$	
Horizontal display timing range	t_{DH}	-	480	-	t_{CPH}	
STV setup time	t_{SUV}	400	-	-	Ns	STVR,STVL
STV hold time	t_{HDV}	400	-	-	Ns	STVR,STVL
STV pulse width	t_{STV}	-	-	1	t_H	STVR,STVL
Horizontal lines per field	t_V	256	262	268	t_H	
Vertical display start	t_{SV}		3	-	t_H	
Vertical display timing range	t_{DV}		234	-	t_H	
VCOM rising time	t_{RCOM}		-	5	Ms	
VCOM falling time	t_{fCOM}		-	5	Ms	
VCOM delay time	t_{DCOM}		-	3	Ms	
RGB delay time	t_{DRGB}		-	1	Ms	

8-5) Signal Timing Waveforms

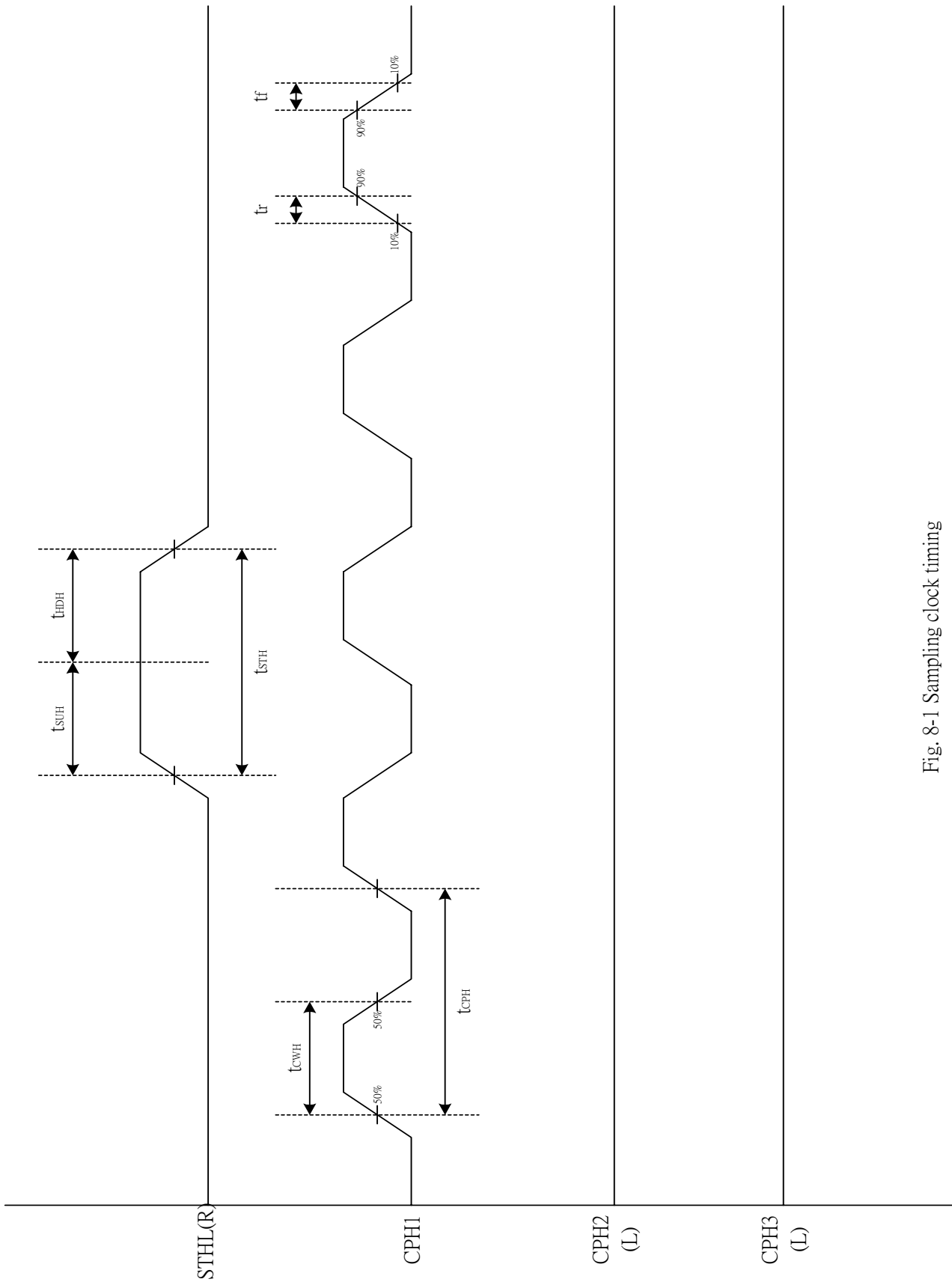


Fig. 8-1 Sampling clock timing

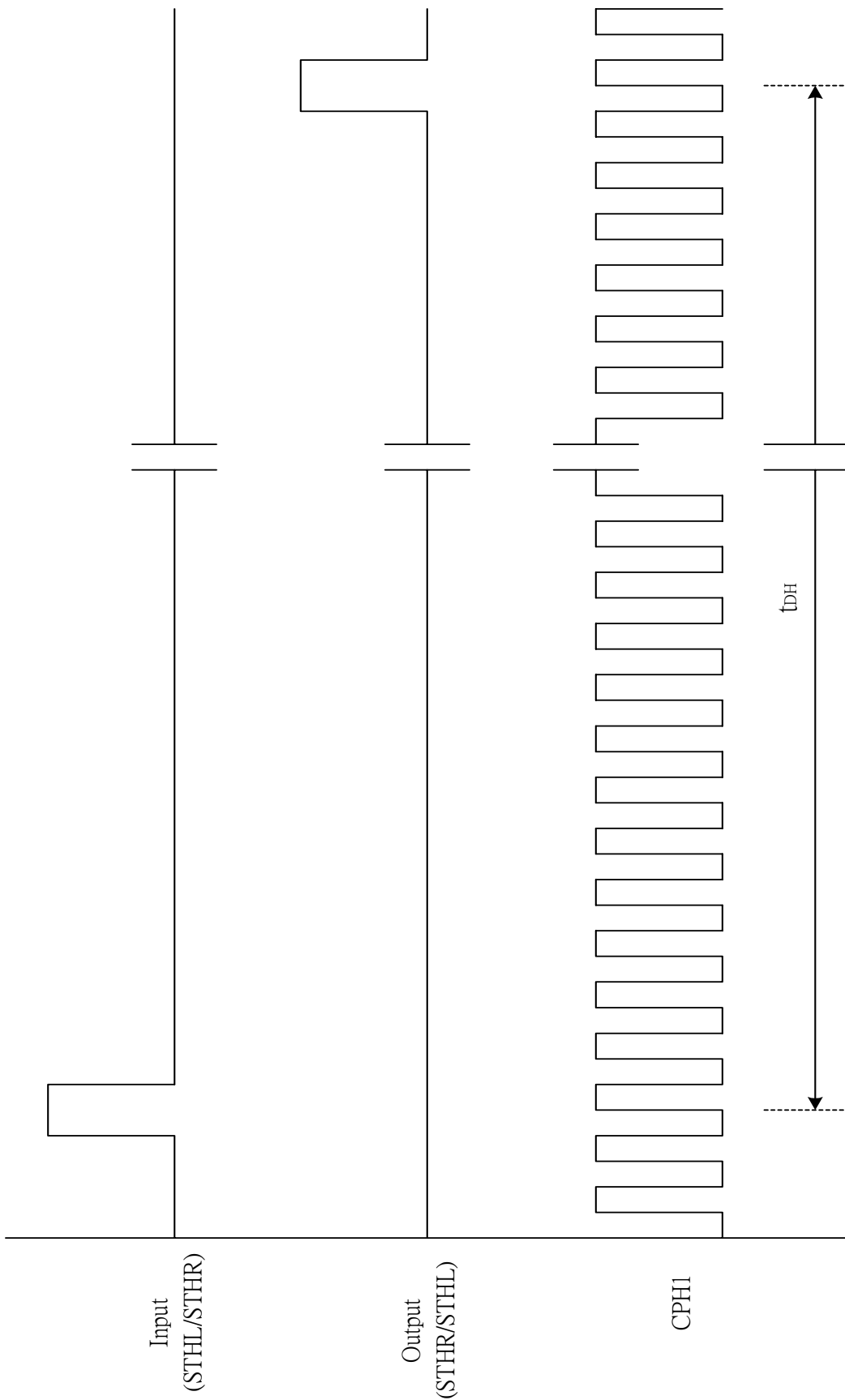


Fig. 8-2 Horizontal display timing range

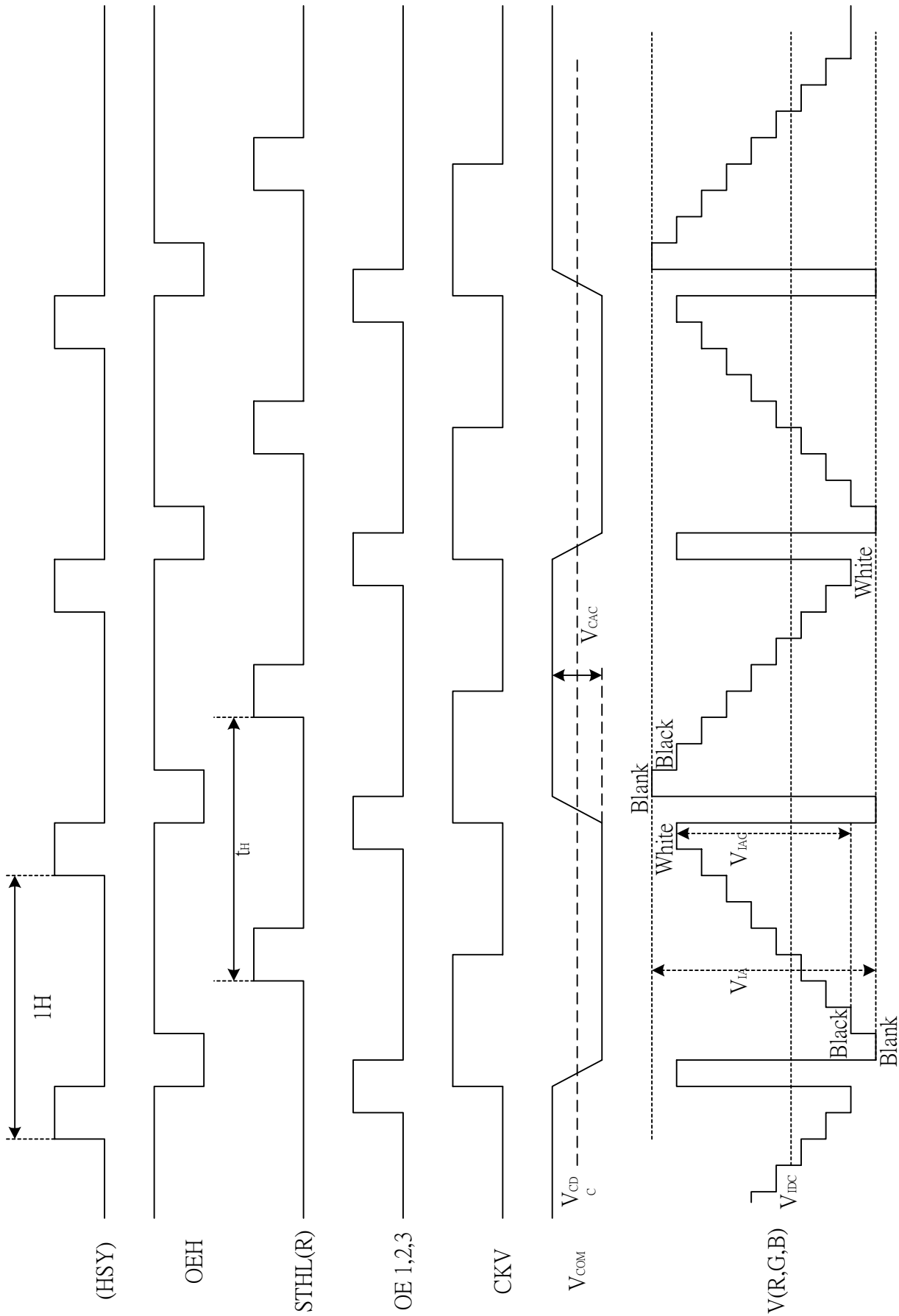


Fig. 8-3 (a) Horizontal timing

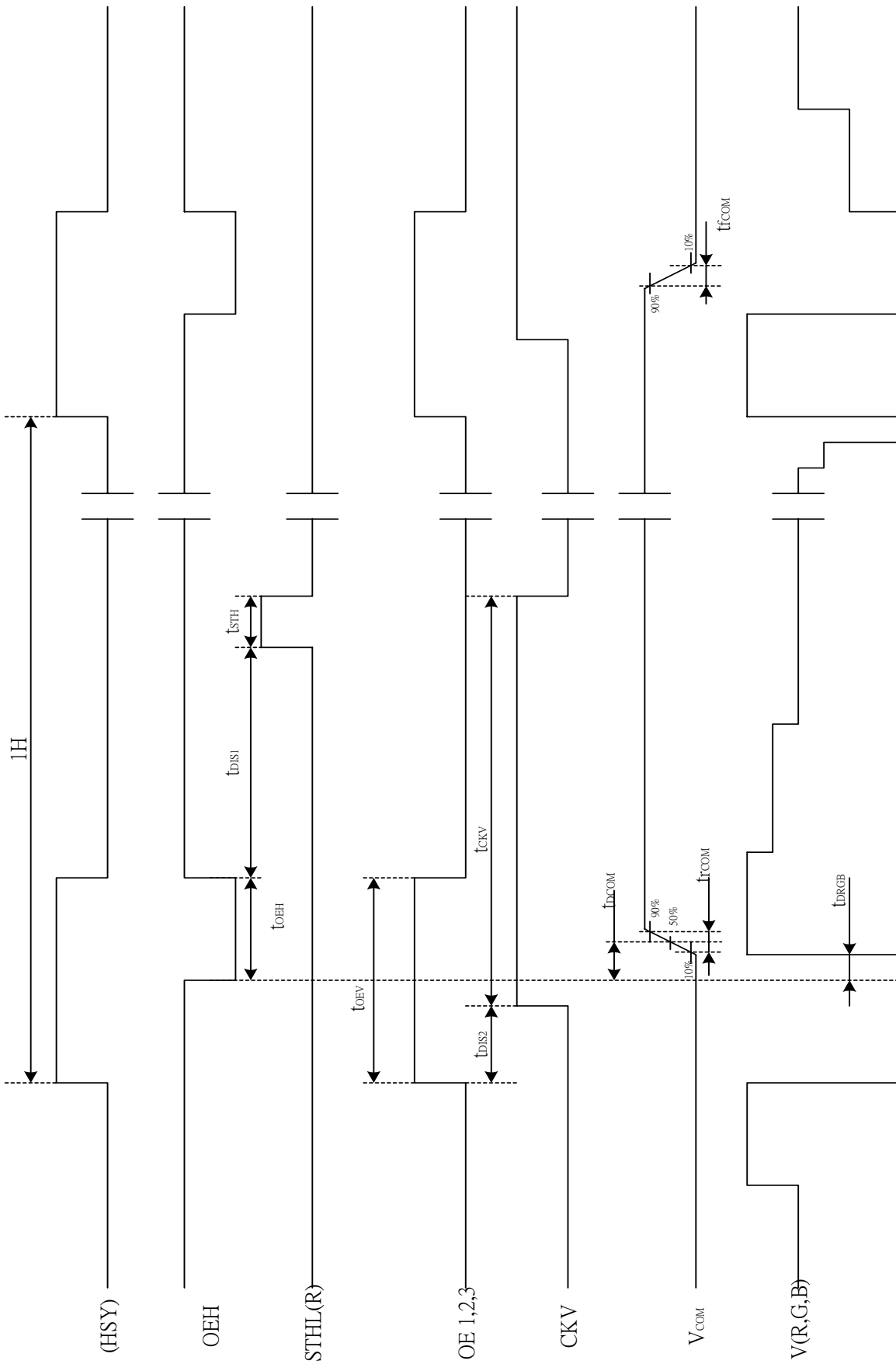


Fig. 8-3 (b) Detail horizontal timing

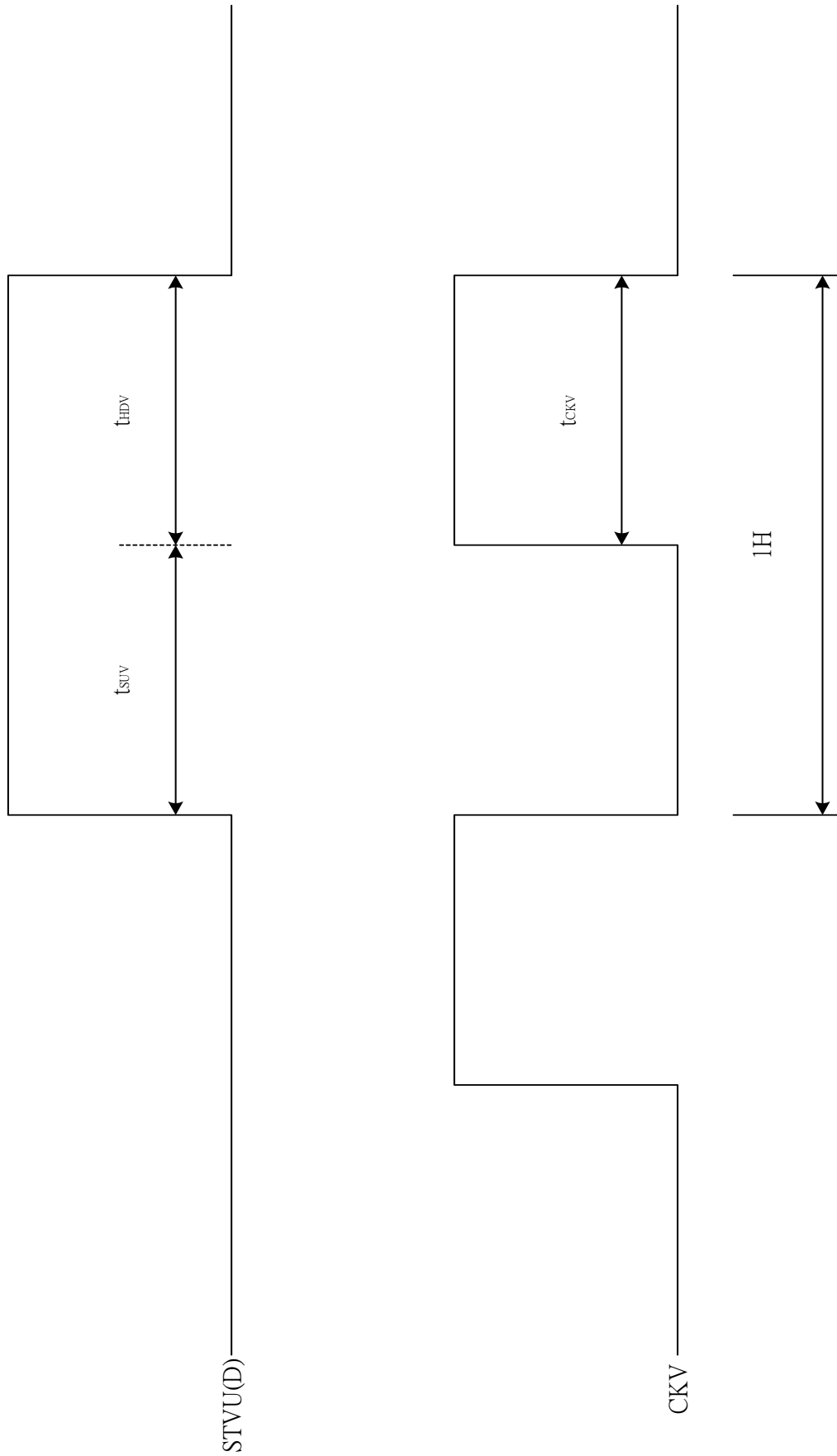


Fig. 8-4 Vertical shift clock timing

Vertical timing (From up to down)

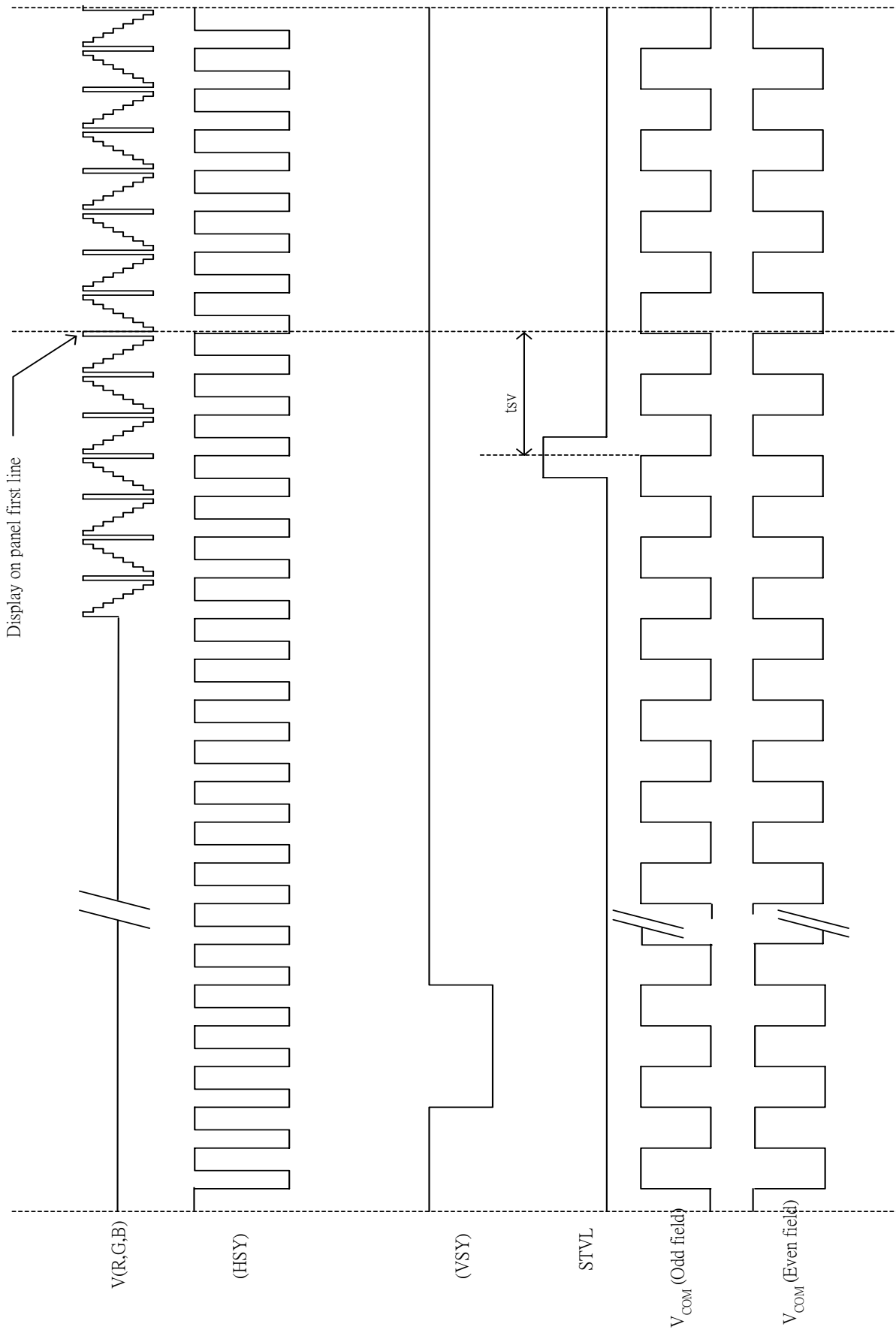


Fig. 8-5 (a) Vertical timing (From Up to Down)

Vertical timing (From down to up)

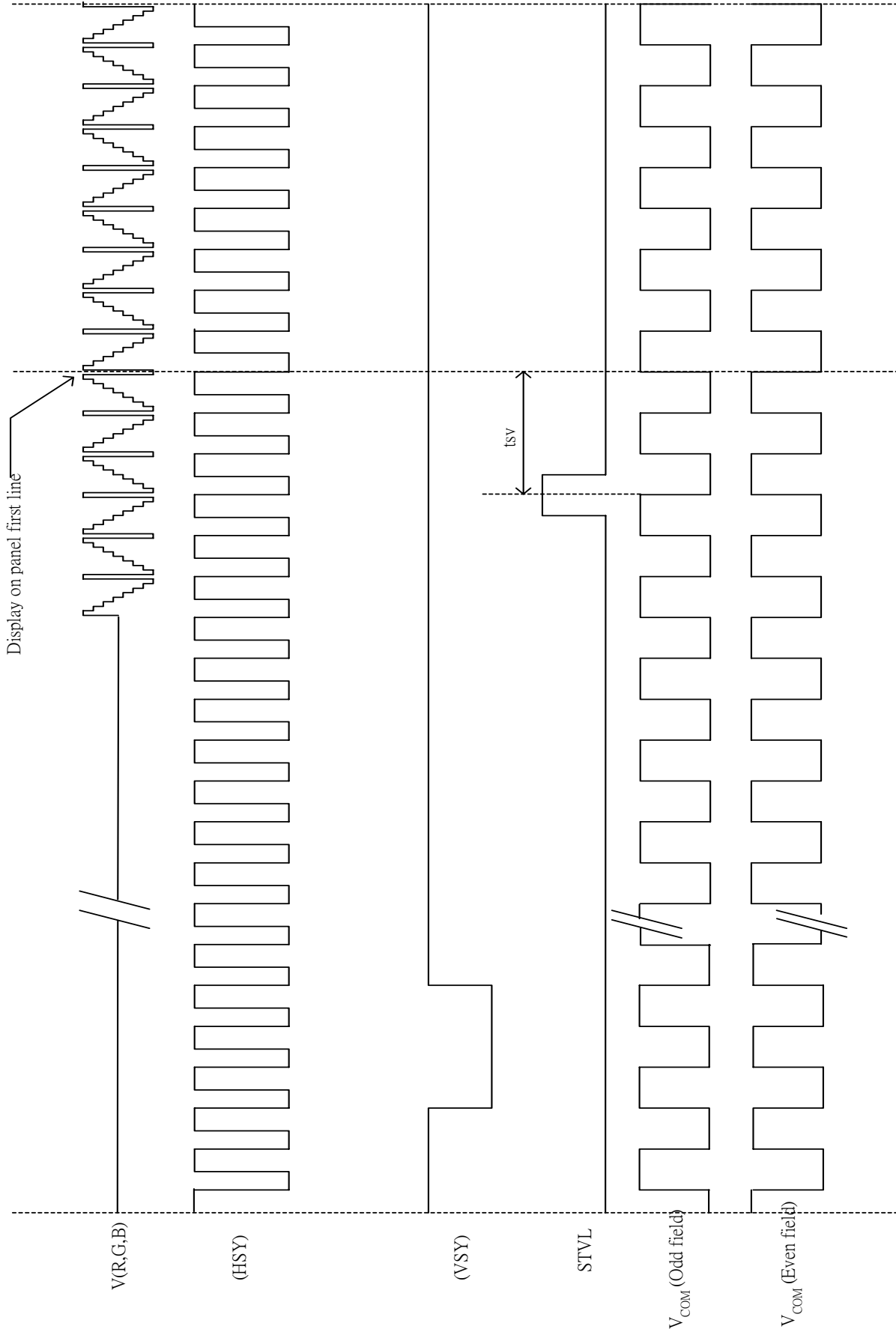
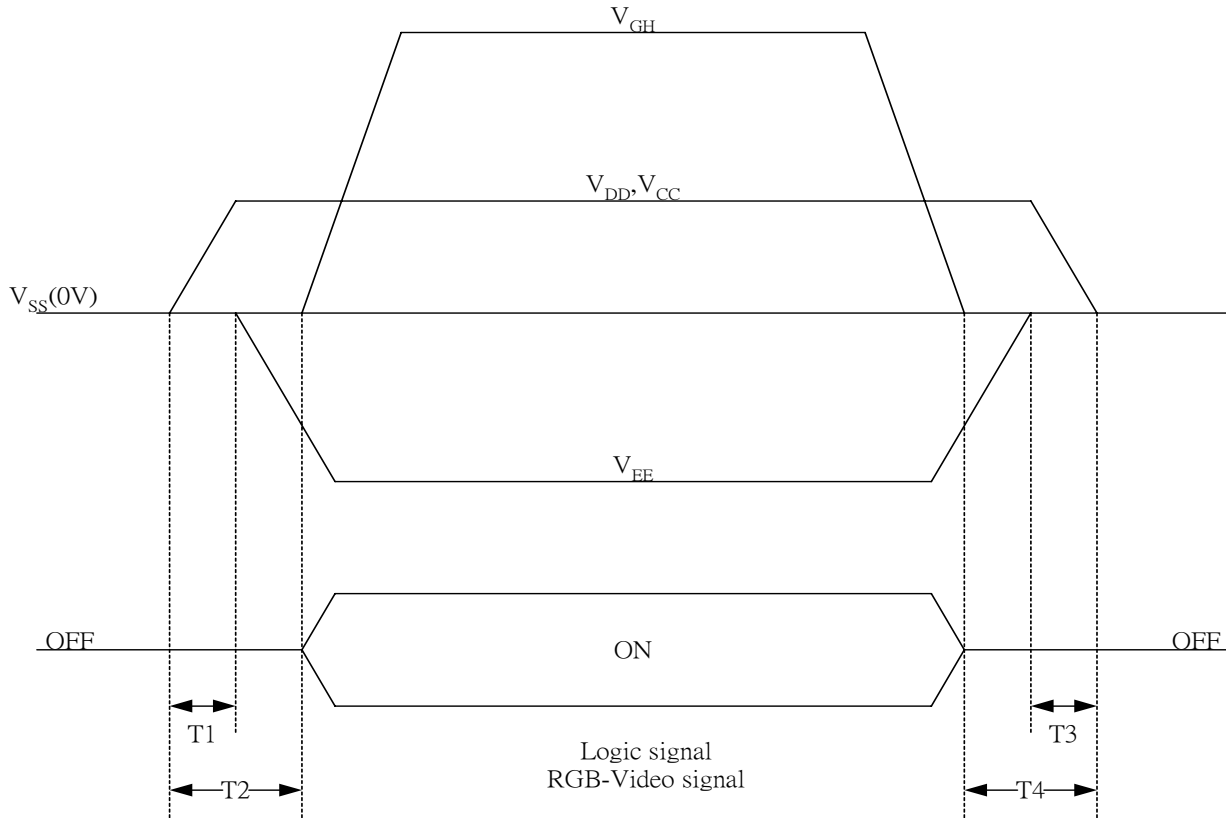


Fig. 8-5 (b) Vertical timing (From Down to Up)

9. Power on Sequence

The Power on Sequence only effect by V_{CC} , V_{DD} , V_{EE} and V_{GH} , the others do not care.



- 1) $10ms \leq T1 < T2$
- 2) $0ms < T3 \leq T4 \leq 10ms$

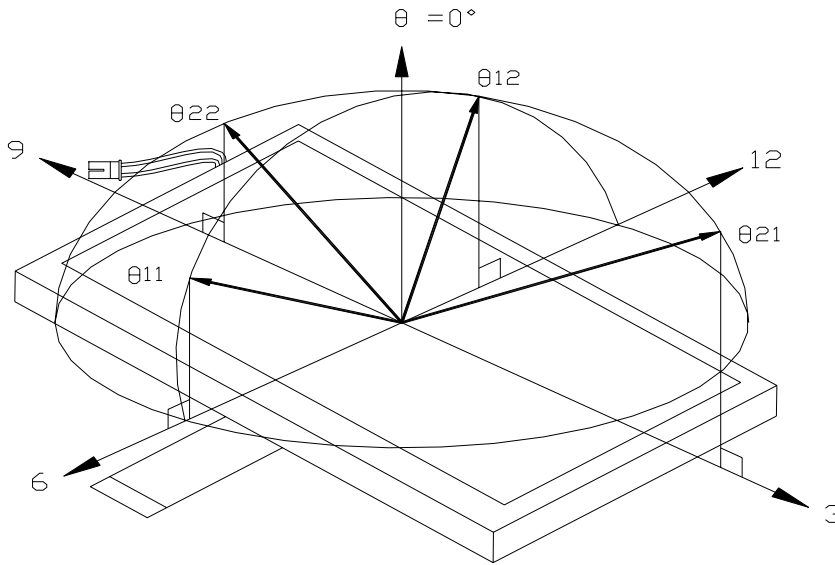
10. Optical Characteristics

10-1) Specification

$T_a = 25^\circ C$

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ_{21}, θ_{22}	55	60		deg	Note 10-1
	Vertical	θ_{12}	35	40		deg	
		θ_{11}	45	50		deg	
Contrast Ratio	CR	At optimized Viewing angle	200	350			Note 10-2
Response time	Rise	T_r		15	30	ms	Note 10-4
	Fall	T_f		25	50	ms	
Brightness			350	400		cd/m ²	Note 10-3
Uniformity	U		70	75		%	Note 10-5
White Chromaticity	x	$\theta = 0^\circ$	0.270	0.300	0.330		Note 10-3
	y		0.297	0.327	0.357		
Lamp Life Time		$+25^\circ C$		30000		hrs	

Note 10-1 : The definitions of viewing angles



Note 10-2 : $CR = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

(Testing configuration see 10-2)

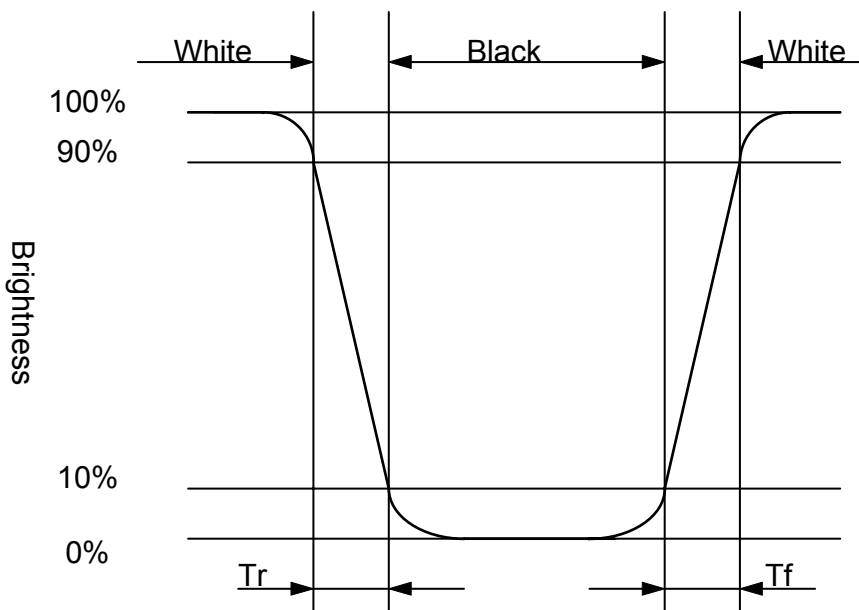
Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : 1. Topcon BM-7(fast) luminance meter 1° field of view is used in the testing (after 20~30 minutes operation).

2.Lamp current : 6 mA

3.Inverter model : TDK-347.

Note 10-4 : The definition of response time:



Note 10-5 : The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

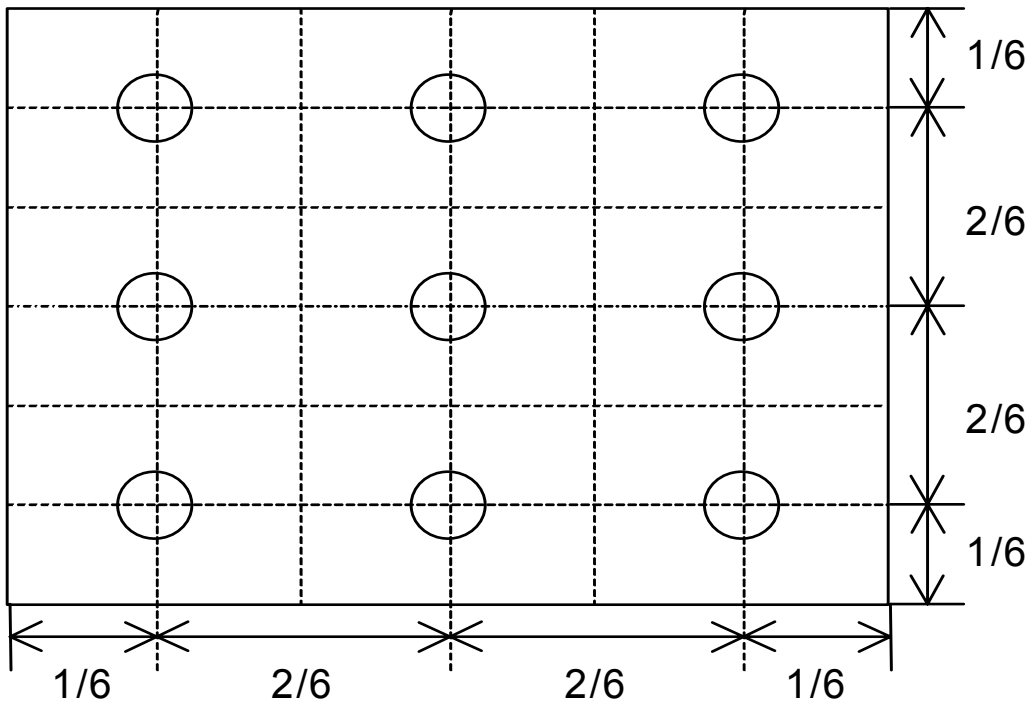
Luminance meter : BM-5A or BM-7 fast (TOPCON)

Measurement distance : 500 mm +/- 50 mm

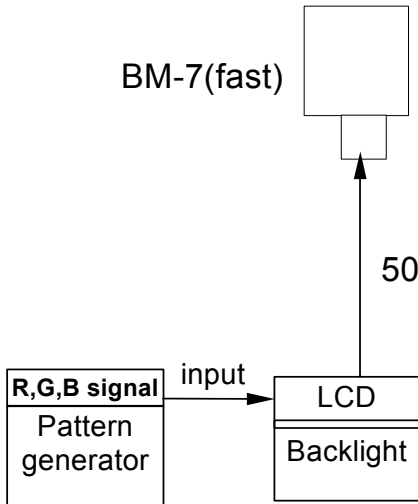
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

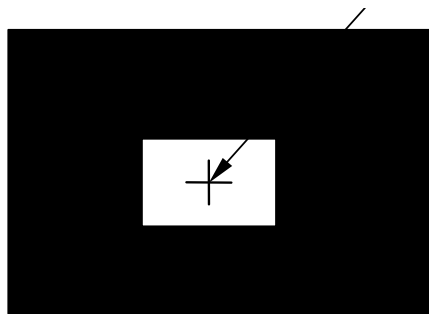


10-2) Testing configuration

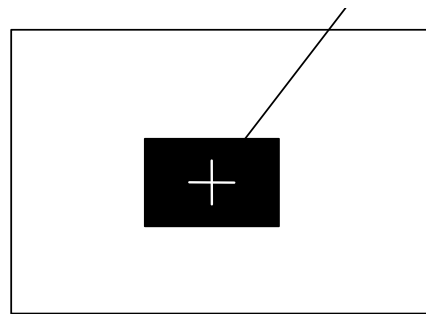


Caution: 1. Environmental illumination ≤ 1 lux
 2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display Testing Point Testing Point

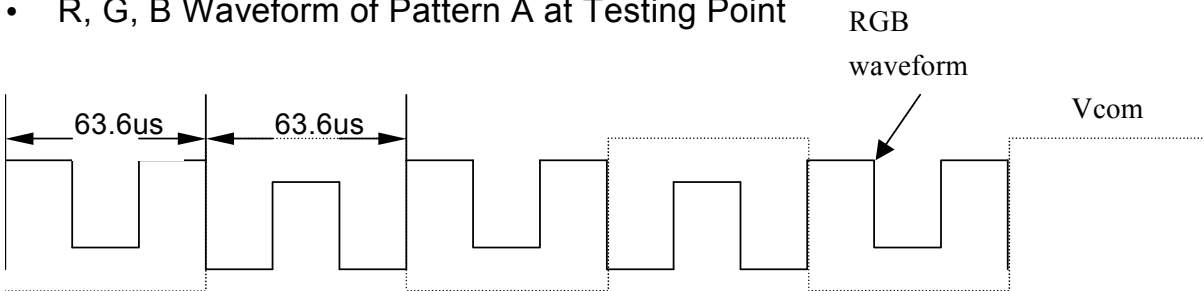


Pattern A

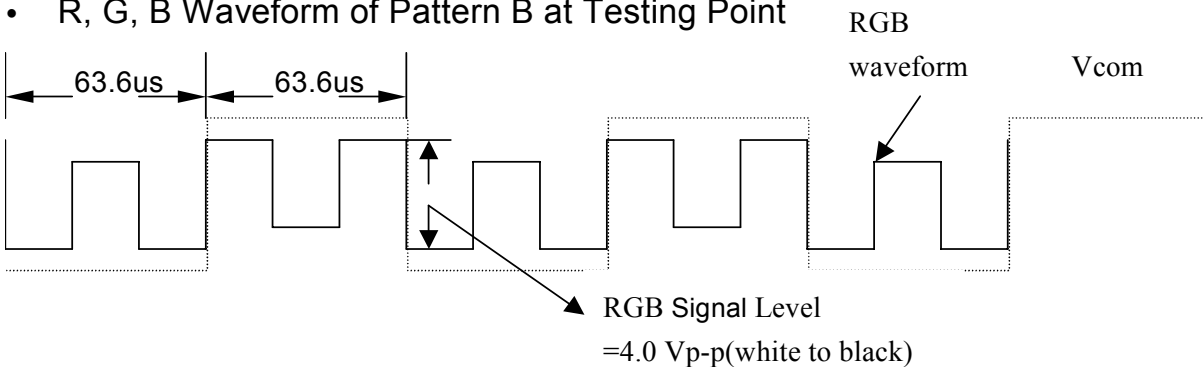


Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



11. Handling Cautions

11-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
 1. The noise from the backlight unit will increase.
 2. The output from inverter circuit will be unstable.
 3. In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.

11-4) Polarizer mark

The polarizer mark is to describe the direction of wide view angle film how to mach up with the rubbing direction.

12. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80°C, 240 hrs
2	Low Temperature Storage Test	Ta = -30°C, 240 hrs
3	High Temperature Operation Test	Ta = +80°C, 240 hrs
4	Low Temperature Operation Test	Ta = -20°C, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60°C, 80%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-30°C→+80°C, 200 Cycles 30 min 30 min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz Amplitude : 1 mm Sweep time: 11 mins Test Period: 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal

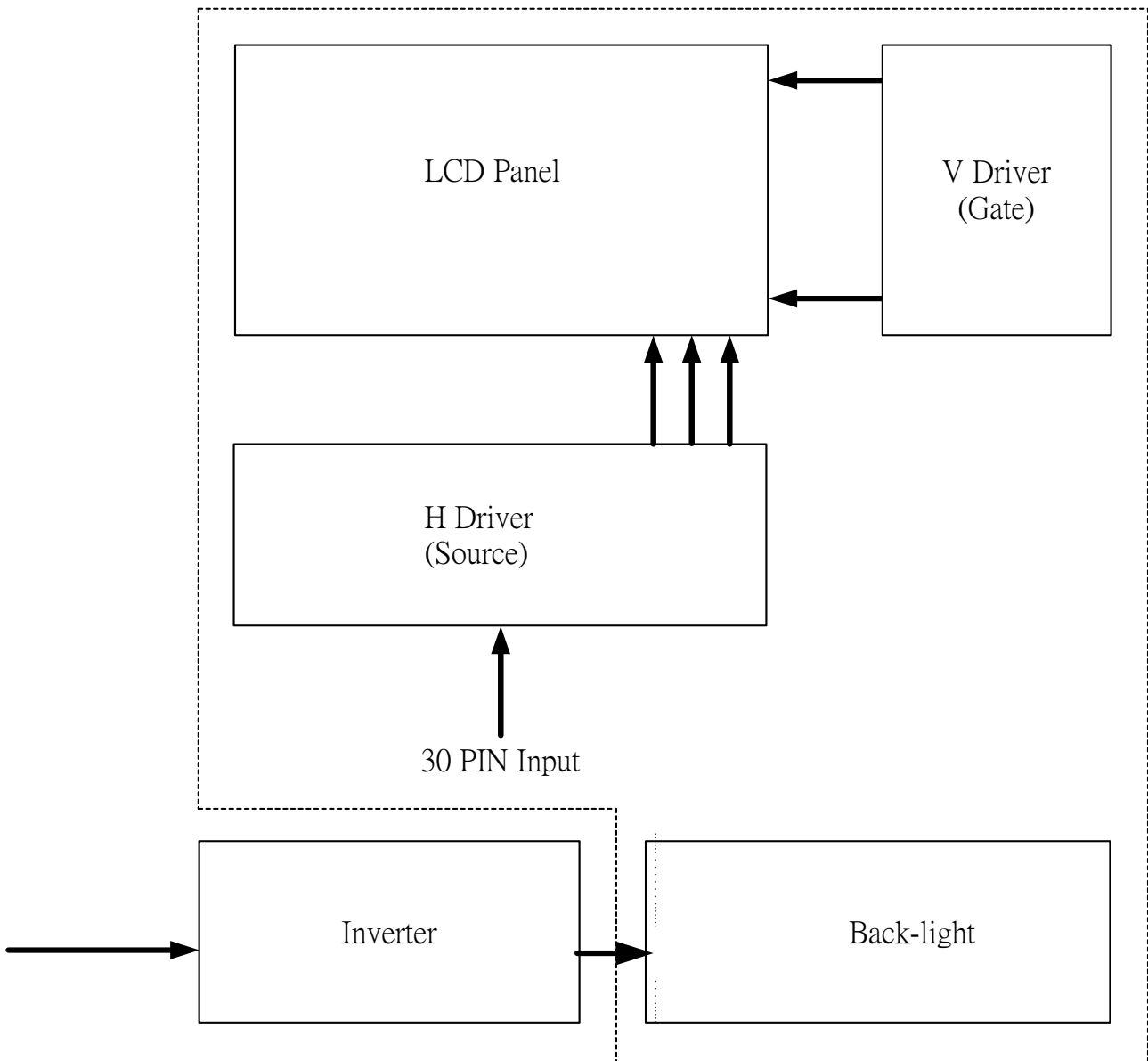
Ta: ambient temperature

Note: The protective film must be removed before temperature test.

[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

13. Block Diagram



Revision History

Rev.	Issued Date	Revised Contents
1.0	Oct. 24, 2003	NEW
1.1	Nov.24, 2003	Modify Page17 : Optical Characteristics (contrast ratio from 150 to 350 Typ.) (contrast ratio from 110 to 200 Min.) Page23: 12. Reliability Test NO.3 Test Item→ Low Temperature Operation Test change to High Temperature Operation Test
1.2	Apr.1,2004	Modify Page4: 4.Mechanical Drawing of TFT-LCD Module (Change ground line form 45mm increase length to 100mm)
1.3	Oct..4,2004	Updata: Page8:Note 8-5 B/L Lamp voltage kick-off time
1.4	Jun.17,2004	Modify Page4: 4.Mechanical Drawing of TFT-LCD Module→FPC change (Two piece FPC band to one piece)