4 MEGABIT (512K × 8)
5 VOLT SECTOR ERASE CMOS FLASH MEMORY

GENERAL DESCRIPTION

The BM29F040 is a 4 Megabit, 5.0 Volts only Flash memory device organized as 512K × 8 bits each. The BM29F040 is offered in an Industry standard 32-pin package which is backward compatible to 1 Megabit and also pin compatible to EEPROMs. The device is offered in PDIP, PLCC and TSOP packages. The device is designed to be programmed and erased in system with the standard system 5 Volt Vcc supply. An external 12.0 Volts Vpp is not required for program and erase operation. The device can also be reprogrammed in standard EPROM programmers.

The BM29F040 offers access times between 70 to 150 nS. The device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls to eliminate bus contention.

BMI flash memory technology reliably stores memory information even after 100,000 erase and program cycles. The BMI proprietary cell technology enhances the programming speeds and eliminates over erase problems seen in the classical ETOX™ type of Flash cell technologies. The combination of cell technology and internal circuit design techniques give reduced internal electrical fields and this provides improved reliability and endurance. The BM29F040 is entirely pin and command set compatible to the JEDEC standard 4 Megabit EEPROM. The commands are written to the Command State machine using standard microprocessor write timings. The internal Programming and Erase Algorithms are automatically implemented based on the input commands.

The BM29F040 is programmed by executing the program command sequence. This will start the internal automatic program Algorithm that times the program pulse width and also verifies the proper cell margin. Erase is accomplished by executing the erase command sequence. The internal Power Switching State Machine automatically executes the algorithms and generates the necessary voltages and timings for the erase operation. The program and erase verify is also done internally and proper margin testing is automatically performed. This scheme unburdens the microprocessor or microcontroller from generating the program and erase algorithms by controlling all the necessary timings and voltages. The entire memory is typically erased in 1.5 seconds. No preprogramming is necessary in this technology.

The BM29F040 also features a sector erase architecture. It is divided into 8 sectors of 64K bytes each. Each sector can be erased individually without affecting the data in other sectors or they can be erased in a random combination of groups. This multiple sector erase capability or full chip erase makes it very flexible to alter the data in BM29F040. To protect the data from accidental program or erase the device also has a sector protect or multiple sector protect function.

The device features a single 5 Volt power supply for read, program and erase operation. Internally generated and well regulated voltages are provided for the program and erase operation. A low Vcc detector inhibits write operations during power transitions. The end of program or erase is detected by Data polling of DQ7 or by the Toggle Bit feature on DQ6. Once the program or erase cycle has been successfully completed, the device internally resets to Read mode.

FEATURES

- 5.0 V +/- 10% Program and Erase
  - Minimizes system power consumption
  - Simplifies the system design
- Compatible with JEDEC standard commands
  - Uses same software commands as EEPROMs
- Compatible with JEDEC-standard byte wide pinout
  - 32 pin PLCC/TSOP
  - 32 pin DIP
- Automated sector/chip Erase Algorithms
  - No programming before Erase needed
  - Internal program and Erase Margin Check
- Data Polling and Toggle Bit
  - useful for detection of Program and Erase cycle completion
- Sector Erase architecture
  - 8 Equal sectors of 64K bytes each
  - Any combination of multiple Sector Erase
  - Full Chip Erase
- Sector Protection
  - Any number of sectors can be protected from Program and Erase operation
- Low Power Consumption
- Typically 100,000 Program/Erase cycles
- Erase Suspend and Resume
  - Suspend the Sector Erase Operation to allow a READ in another sector
- Low Vcc Write inhibit < 3.2 volts
- Single Cycle reset command

Product Selection Guide

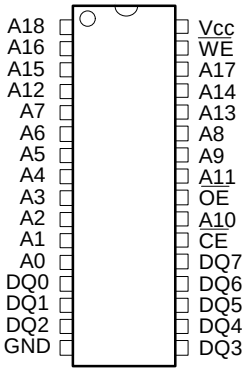
FAMILY PART NO.	-75*	-90	-120	-150
Maximum Access Time (nS)	70	90	120	150
$\overline{CE}$ (E) Access time (nS)	70	90	120	150
$\overline{OE}$ (G) Access time (nS)	30	35	50	60

Table 1

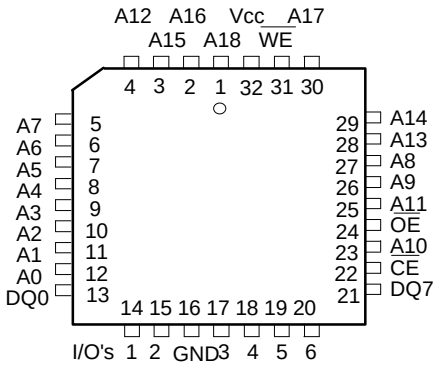
*This speed is available with Vcc = 5V +/- 5% variation

PIN CONFIGURATIONS

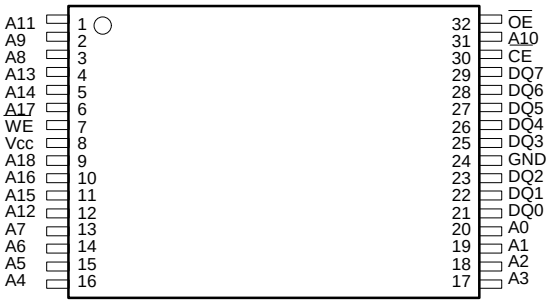
DIP Top View



PLCC Top View



TSOP Top View
TYPE 1



Flexible Sector-erase Architecture:

64K bytes per sector
Individual sector, multiple sector or bulk erase capability.
Individual or multiple-sector protection is user definable.

Table 2. Sector Definition

64K byte sector	70000H-7FFFFH
64K byte sector	60000H-6FFFFH
64K byte sector	50000H-5FFFFH
64K byte sector	40000H-4FFFFH
64K byte sector	30000H-3FFFFH
64K byte sector	20000H-2FFFFH
64K byte sector	10000H-1FFFFH
64K byte sector	00000H-0FFFFH

PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
A_0 - A_{18}	I	**ADDRESS INPUTS**: for memory addresses. Addresses are internally latched during a write cycle.
A_9	I	**ADDRESS INPUT**: When A_9 is at 12 Volts the ID mode is accessed. During this mode A_0 decodes between the manufacturer and device ID's.
DQ_0-DQ_7	I/O	**DATA INPUTS / OUTPUTS**: Inputs array data on the fourth $\overline{CE}$ and $\overline{WE}$ cycle during a program command. Inputs commands $\overline{WE}$ to the Command register when $\overline{CE}$ and $\overline{WE}$ are active. Data is internally latched during the program cycles. Outputs are from Array and Intelligent Identifier information. The output pins float to tri-state when the chip is deselected or the outputs are disabled.
$\overline{CE}$	I	**CHIP ENABLE**: Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low control; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	I	**OUTPUT ENABLE**: $\overline{OE}$ is active low control signal. This pin gates the device's outputs through the data buffers during a read cycle. When $\overline{CE}$ is low and $\overline{OE}$ is high the outputs are tri-state.
$\overline{WE}$	I	**WRITE ENABLE**: Controls writes to the Command state Machine and memory array. $\overline{WE}$ is active low signal. Addresses and Data are latched during the rising edge of the $\overline{WE}$ pulse.
Vcc		**DEVICE POWER SUPPLY**: Main power source to the device. It's value is 5V ± 10% or 5V ± 5%.
GND		**GROUND**: The device ground for the internal circuitry.

Table 3

BLOCK DIAGRAM

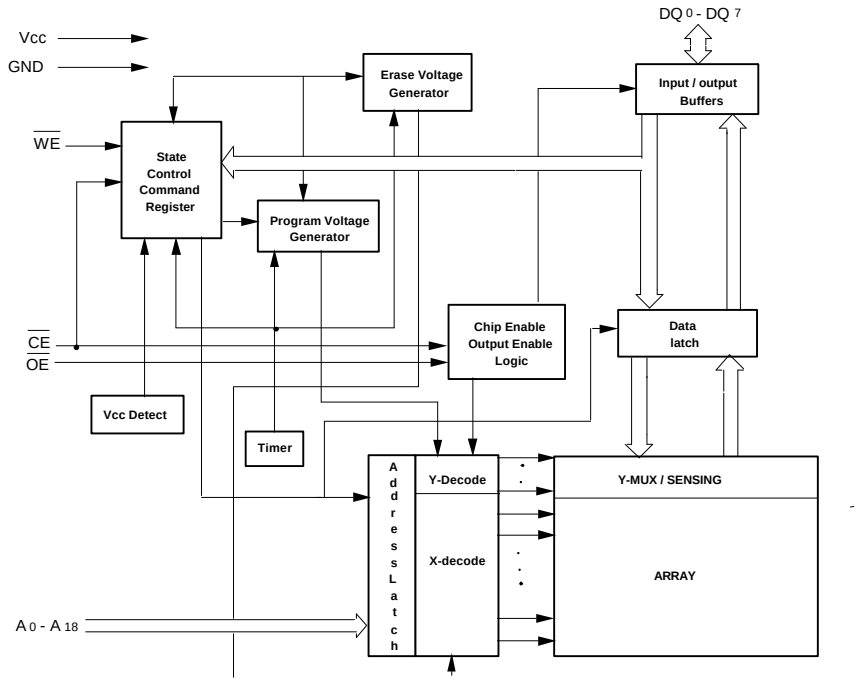


Figure 1

BUS OPERATION

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	I/O
Auto select Manufacturers ID (1)	L	L	H	L	L	L	V_{ID}	Code
Auto select Device ID (1)	L	L	H	H	L	L	V_{ID}	Code
Read	L	L	H	A0	A1	A6	A9	Dout
Standby	H	X	X	X	X	X	X	High Z
Output Disable	L	H	H	X	X	X	X	High Z
Write	L	H	L	A0	A1	A6	A9	Din (2)
Enable Sector Protect	L	V_{ID}	L	X	X	X	V_{ID}	X
Verify Sector Protect (3)	L	L	H	L	H	L	V_{ID}	Code

Table 4

Notes:

1. LEGENDS: L = V_{IL}, H = V_{IH}, X = don't care, V_{ID} = +12V.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to table 6 for Command definitions.
3. Refer to Table 4 for valid Din during a write operation.
4. Refer to the section on sector protection.

Autoselect Codes

TYPE	A_{18}	A_{17}	A_{16}	A_6	A_1	A_0	Code (Hex)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	X	X	X	Vil	Vil	Vil	ADH	1	0	1	0	1	1	0	1
BM29F040 Device code	X	X	X	Vil	Vil	Vih	40H	0	1	0	0	0	0	0	0
Sector Protection (1)	Sector Addresses			Vil	Vih	Vil	01H	0	0	0	0	0	0	0	1

Table 5

PRODUCT FAMILY PRINCIPLES OF OPERATION

Flash memory devices are electrically alterable non-volatile memory products. The BM29F040 augments this feature by not requiring an additional Vpp power supply. The 4 Megabit flash family uses a Command register and internally generated voltages and timing algorithms to make program and erase operations simple. The user need not worry about generating tightly controlled high voltages on board or tying up the microcontroller to generate program and erase algorithms.

The Command register allows for 100% TTL-level control inputs, and maximum compatibility with the Flash memory functions.

The device provides standard EPROM read, standby and output disable operations. Manufacturer Identification and Device Identification data can be accessed through the Command register or through the standard EPROM ″A9″ high voltage access (V_{ID}) for PROM programming equipment.

A Command register and Power Switching State Machine are built inside the device. Their purpose is to completely automate the program and erase operation. The command register receives the commands given by the user and internally controls the power switching state machine.

Read Mode

The BM29F040 has three control pins and they should all be logically active to obtain valid data at the outputs. Chip-Enable ($\overline{CE}$) is the device selection control. Output Enable ($\overline{OE}$) is the data input/output control. This pin when high (V_{IH}) brings the output drivers to the tristate and allows data into the device. Data input is then controlled by $\overline{WE}$. When the $\overline{OE}$ pin is low (V_{IL}) it enables the output buffers and valid array data becomes available at the output pins. The Write Enable ($\overline{WE}$) pin has to be high during the READ mode.

Standby Mode

The BM29F040 has two standby modes: a CMOS standby mode ($\overline{CE}$ input = Vcc +0.5V) when the current consumed is less than 100 μA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current consumed is approximately 1 mA. In the standby mode the outputs are in a high impedance state independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the erase or programming operation is complete.

Autoselect Mode

The Autoselect mode allows access to the manufacturers and the device code. This mode can be enabled by either taking the address pin A9 to V_{ID} (11.5 to 12.5 volts) or by giving the Autoselect Command sequence as shown in Table 5. Once the Autoselect mode is enabled two identifier bytes can be read on the device outputs by toggling A0 from V_{IL} to V_{IH}. Byte 0 (A0 = V_{IL}) represents the manufacturers code (ADH for BMI). Byte 1 (A0 = V_{IH}) represents the device identifier and this is 40H for the BM29F040. A READ command must be written to the Command register to return to the Read mode after the Autoselect mode.

Write Operations

The on-chip state machines control the Chip Erase, Sector Erase and byte Write operations. This frees the system processor to do other tasks. All the Programming and Erase voltages are generated internally. The Write and Erase timings and algorithms are also built into the device. The byte write/ sector erase or Chip Erase Command Interface provides additional data protection to avoid accidental Write or Erase.

Commands are written to the Command register using standard microprocessor write timings. The Command register recognizes Read mode, Autoselect mode, Chip Erase, Sector Erase (64K bytes per sector) and Program commands. The Command register does not occupy an addressable memory location. The interface register is a latch used to store the command and address and data information needed to execute the command.

Command Definitions

Device operations are selected by writing specific address and data sequences into the Command register. Table 6 defines these Command sequences.

Read/ Reset Command

The read or reset operation is initiated by writing the read/reset command sequence to the command register. Processor read cycles retrieve the data from the memory. The device remains enabled for reads until the command register contents are changed.

The device will automatically power-up in the read/reset mode. In this case, a command sequence is not needed to read the memory data. This default power up to read mode ensures that no spurious changes of the data can take place during power-up. As shown in this data sheet, the timing parameters and A.C. read waveforms should be referenced.

A single cycle reset is also available as shown in table.

Table 6. Command Definitions

Command Sequence	Bus Write cycles required	First Bus Write cycle		Second Bus Write cycle		Third Bus Write cycle		Fourth Bus Write cycle		Fifth Bus Write cycle		Sixth Bus Write cycle	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read /Reset	1	XXXXH	F0H										
Read /Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Auto Select	4	5555H	AAH	2AAAH	55H	5555H	90H	00H	ADH				
								01H	40H				
Auto Select Sector Protect Verify	4	5555H	AAH	2AAAH	55H	5555H	90H	SA	00				
								X02	01				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend	1	XXXXH	B0H										
Sector Erase Resume	1	XXXXH	30H										

Notes:

1. Address bit A15, A16, A17 and A18 = X = don't care for all address commands except for Program address (PA) and sector address (SA).
2. Bus operations are defined in Table 4.
3. RA = Address of the memory location to be read. PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of WE. SA = Address of the sector to be erased. The combination of A16, A17 and A18 will uniquely select the sector.
4. RD = Data from the selected address location (RA) during read operation. PD = Data to be programmed at the selected memory location (PA). Data is latched at the falling edge of /WE.
5. Auto select command can be used to evaluate whether a block is protected or not by using at the fourth address 02H. This is similar to placing A9 to High Voltage.

Auto Select Command

The BM29F040 contains two different procedures for the autoselect mode. One is the traditional PROM programmer methodology (by taking Address pin A9 to V_{ID}) and the other is by writing the Auto Select command sequence into the command register. Following the third bus cycle write command, a read cycle from Address 00H retrieves the BMI manufacturer code ADH, and a read cycle at 01H retrieves the device code of 40H. Scanning the sector addresses (A16, A17, A18) while (A6, A1, A0) = (0, 1, 0) will produce a logical at device output DQ0 for a protected sector. See table 5 for more details.

To terminate this operation, it is necessary to write the read/ reset command to the command register.

Byte Write or Byte program

The BM29F040 is programmed one byte at a time. Programming is a four bus cycle operation. There are two "unlock" write cycles which are followed by a program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. The rising edge of $\overline{WE}$ begins programming. During the execution of the embedded program algorithm the host system is not required to provide any other controls or timings. The device also provides adequate program margin and all the necessary voltages and timings. When completed, the automatic programming will provide the equivalent of the written data on DQ7. After a successful programming
operation the device returns back to read mode. Data polling must be performed at the memory location which is being programmed.

Figure 3 illustrates the Embedded Programming Algorithm and the waverforms are shown in figures 9 and 10.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the ″setup″ command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. BM29F040's technology is immune to overerase and it does not need any internal programming algorithm before erase. This can save erase time in many applications.

The automatic Chip erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1", and which time the device returns back to the read mode.

Figure 4 illustrates the Auto Erase Algorithm and the Erase Waveforms are shown in Figure 11.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles followed by writing the sector erase setup command. Two more "unlock" write cycles are then followed by the sector erase confirm command. The sector address is latched on the failing edge of $\overline{WE}$, and the command data is latched on the rising edge of $\overline{WE}$. An 80 μS time-out from the rising edge of $\overline{WE}$ of the last sector erase command is initiated. The actual sector erase starts 100 uS after the last rising edge of $\overline{WE}$.

Multiple sectors can be erased simultaneously. After writing the six bus cycle command for sector erase additional sector address and sector erase command can be inserted within the 80 uS time-out period. The timer is reset every time and additional sector erase command is inserted. The sectors can be added to be erased in any random sequence. Any command other than the sector erase command or Erase Suspend command during the time-out period will reset the device to the read mode and ignoring the previous command string. During the execution of the Sector Erase command, only the Erase Suspend and Erase Resume commands are allowed. All other commands will reset the device to the Read mode. Once the device resets to the Read mode due to command error during Sector Erase, the data in this sector has lost its integrity. The sector should be properly erased again.

Sector erase does not require the user to program the sector before erase. When erasing a sector or multiple sectors the data in the unselected sectors remains unchanged. After the sector erase

operation is completed the data on DQ7 becomes "1", and the device returns to the read mode. Data polling must be performed at an address within any of the sectors being erased.

Figure 4 shows the Embedded Erase Algorithm and Figure 11 shows the Sector Erase Waveforms.

Erase Suspend and Resume

The Erase suspend command allows the user to interrupt the sector erase function and then read data from the other sectors which were not being erased. This command is not applicable during the Chip erase operation or during the program mode. The Erase suspend command (B0H) will terminate the Sector erase operation and it may require form 0.1 μS to 70 μS to suspend the erase operation and go into the read mode (pseudo read mode). The user must use the toggle bit to determine if the chip has entered the erase suspended read mode, at which time the toggle bit will stop toggling. An address of a sector not being erased must be used to read the toggle bit. The user must keep the information whether the device is in pseudo read mode or read mode. Every time an Erase suspend command followed by an Erase resume command is written the internal counters are reset. The erase suspend command is allowed during the 100 μS time out window before the actual sector erase operation starts. The Erase resume command will start the erase operation immediately and there is no time out window during erase resume. Note that any other command during the time out will reset the device to read mode.

To resume the Sector erase operation after pseudo read mode the Resume command (30H) should be written. The sector erase will start immediately. Another Erase suspend command can be written after the chip has resumed the erase operation. Note that a data "0" can not be programmed back to "1." Attempting to do so may give erroneous results or may hang up the device. Only an erase operation can change the data from a "0" to "1".

The system may also write the Autoselect Command during the Erase Suspend mode. This allows the host system to correctly read the autoselect codes during Erase Suspend since this data is not stored in the memory array.

Sector Protection

The BM29F040 has a hardware sector protection. This feature will disable both Program and Erase operation of the protected sector or group of sectors. The device is shipped with all sectors unprotected.

To verify if a sector is protected, the programming equipment must force V_{ID} on the address pin A9, and A6 = $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{WE}$ = V_{IH}. Reading the device at a particular sector address (A16, A17 and A18) and XXX2H will produce 01H at the data outputs for a protected sector. See Figure 14 for the AC Waveforms and Figure 16 for the algorithm.

Please use the appropriate approved Programmer or contact Bright for the BM29F040 Programmers Guide for the specification for protecting individual sectors.

Sector Unprotection

The BM29F040 also features a sector unprotect mode, so that a protected sector may be unprotected. All sectors are unprotected at the same time. Please use the appropriate approved Programmer or contact Bright for the BM29F040 Programmers Guide for the specification to unprotect the sectors.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set to V_{IH}. Performing a read operation at XXX2H and the sector address (defined by A16, A17 and A18) will produce 00H at the Data outputs for an unprotected sector.

Table 7 Sector Address Table

Sector	A18	A17	A16	Address Range
SA0	0	0	0	00000H - 0FFFFH
SA1	0	0	1	10000H - 1FFFFH
SA2	0	1	0	20000H - 2FFFFH
SA3	0	1	1	30000H - 3FFFFH
SA4	1	0	0	40000H - 4FFFFH
SA5	1	0	1	50000H - 5FFFFH
SA6	1	1	0	60000H - 6FFFFH
SA7	1	1	1	70000H - 7FFFFH

Data Flags

DQ7 Data polling

The BM29F040 features Data polling to indicate to the host system that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the Data last written to DQ7. Upon completion of the Embedded Programming Algorithm an attempt to read the device will produce the true data last written to DQ7. Data polling is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence.

During the Embedded Erase Algorithm, DQ7 will be "0" until the Erase operation is completed. Upon completion of Erase the data at DQ7 is "1". For sector erase, the Data polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. For Chip erase, the Data polling is valid after the last rising edge of the sixth Chip erase $\overline{WE}$ pulse. Data polling must be performed at a sector address within any of the sectors being erased and not a protected sector. Once the Embedded operation is close to being completed, the BM29F040 data pins (DQ7) may change asynchronously while the $\overline{OE}$ pin is asserted low. This means that the device is driving status information on DQ7 at one time and bytes of valid data at other times. Depending on when the system samples the DQ7 output it may read the status or it may read the valid data.

See Figure 12 for the Data polling timing diagram.

DQ6 Toggle Bit

The BM29F040 also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read data from the device will result in DQ6 toggling between "1" and "0". Once the Embedded Program or Erase algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on successive attempts. During programming the toggle bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. During Chip and Sector Erase, the toggle bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence.

In programming, if the sector being written to is protected, the toggle bit may toggle for about 2 μS and then will stop toggling without the data being changed. During erase the device will erase all the sectors except the sector being protected. If all the sectors are protected the chip will toggle the toggle bit for about 2 μS and then drop back to read mode without changing the data.

Either $\overline{CE}$ or $\overline{OE}$ toggling will cause the DQ6 to toggle. The toggle bit is valid in the time out period during sector erase.

See Figure 13 for the Toggle bit timing diagrams.

DQ5 Exceeded The Timing Limits

DQ5 indicates if the program or erase time has exceeded the specified timing limits. Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions. The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable function as shown in Table 4.

If this failure condition occurs during the sector erase operation, it indicates that the particular sector is bad and may not be reused. The other sectors are still functioning properly and can be used. The device must be reset to use the other good sectors. To reset the device, write the Reset command sequence to the device. This will allow the system to use the other active sectors in the device.

If this failure condition occurs during chip erase, it indicates that the entire chip is bad or many sectors are bad.

If this condition occurs during byte write it indicates that the sector containing this byte is bad.

This failure condition can also occur if the user tries to program a non-blank location without erasing. In this case the device locks out and never completes the operation. Please note that this is not a device failure.

DQ3 Sector Erase Timer

After the completion of the Sector erase command sequence the sector erase time-out begins. DQ3 will remain low until the time-out is complete. Data polling and the Toggle bit are valid after the initial sector erase command sequence.

If Data polling or the Toggle bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is "1" the internally controlled erase cycle has begun. If DQ3 is "0" the device will accept additional sector erase commands. To ensure that the command has been accepted, the user should check the status of DQ3 prior to and following each sector erase command. If DQ3 is "1" on the second status check, the command may not be accepted.

Once the internal erase cycle begins the device will not accept any other command until the internal erase cycle is completed.

The BM29F040 is designed to offer protection against accidental programming or erasure. During power-up the device automatically resets to the read mode. The multi-bus command sequences also provide data protection for accidental write. The device also provides additional features to prevent inadvertent write operations during power-up and power-down transitions or system noise.

DQ2 Toggle Bit II

The BM29F040 also features the "Toggle Bit II" as a method to indicate to the host system whether a specific sector is actively erasing or whether the sector is erase-suspended. The Toggle Bit II is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence.

DQ2 toggles when the host system reads addresses within a sector that have been selected for erase. The system may use $\overline{OE}$ or $\overline{WE}$ to control the read cycles. But, DQ2 can not distinguish between a sector erasing or erase-suspended. However, Toggle Bit DQ6 can be used to determine if a sector is actively erasing or erase-suspended. As a result, both Toggle Bits are required for the host system to determine the current mode information. Refer to Table 7 for a further comparison of DQ6 and DQ2.

Whenever the host system begins to read the erase status using the toggle bits, they must be read at least twice in a row. Typically, the system would store the first value and compare it to the second. If the bits are still toggling, the system should also check DQ5(see the DQ5 description).

If DQ5 is high, the system should re-check the toggle bits since toggling may have just finished. If the toggle bits have stopped toggling, the device has successfully completed the erase. If the toggle bits are still toggling, the device has not successfully completed the erase operation and the host should issue a Reset Command to the device before continuing.

If DQ5 is low, the host system should continue to monitor the toggle bits and DQ5 or issue an erase suspend command if performing a single or multiple sector erase command.

Write Operation Status

Status		DQ7	DQ6	DQ5	DQ3	DQ2
Standard	Auto-Programming	$\overline{DQ7}$	Toggle	0	N/A	No Toggle
	Auto-Erase	0	Toggle	0	1	Toggle
Erase Suspend	Reading an Erase Suspended Sector	1	No Toggle	0	N/A	Toggle
	Reading a Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Auto-Programming Erase Suspend	$\overline{DQ7}$	Toggle	0	N/A	N/A
Exceeded Time Limits	Auto-Programming	$\overline{DQ7}$	Toggle	1	1	Reserved for Future use
	Auto-Erasing	0	Toggle	1	1	

Table 8. Hardware Sequence Flags

Low Vcc Write Inhibit

During Vcc power-up or power-down, a write cycle is inhibited for Vcc values of less than 3.2 Volts (3.8 Volts typical). If Vcc < Vlko (Vlko = lock out Voltage) the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. If a write command is given during Vcc < Vlko, the writes will be ignored. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc > Vlko.

Write Pulse Glitch Protection

Noise pulses of less than 5 nS on $\overline{OE}$, $\overline{WE}$ or $\overline{CE}$ will not initiate a write cycle.

Power-up Wtire Inhibit

Power-up of the device with $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} will not accept commands at the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Logical Inhibit

Writing is inhibited by holding any one of the control pins to $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} or $\overline{CE}$ = V_{IH}. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be logical "0" and $\overline{OE}$ must be logical "1".

Sector Protect

Sectors of the BM29F040 may be hardware protected by the user. The protection circuitry will disable both program and erase functions for the protected sectors. The program and erase commands will be ignored if given to the protected sectors. The Chip erase command will also not erase the protected sectors.

Parallel Device Erasure

The BM29F040 is a fully self timed device. This makes it feasible to Erase or Program many devices in parallel.

Program Command Sequence (Address/Data)

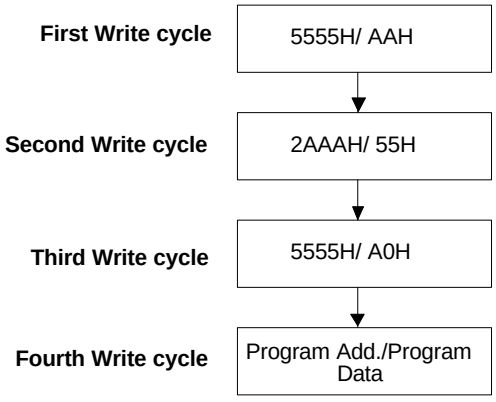


Figure: 3A

Embedded Programming Flow Chart

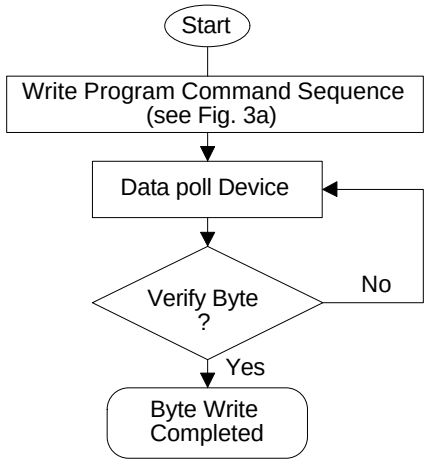


Figure: 3B

Note: See Data Polling Algorithm in Figure 10 and 11.

Embedded Erase Algorithm

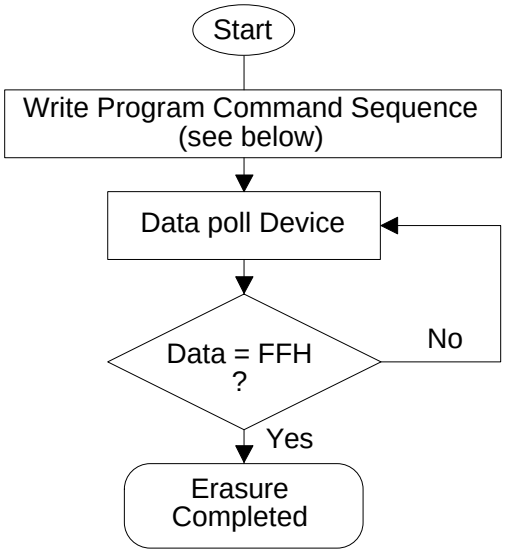
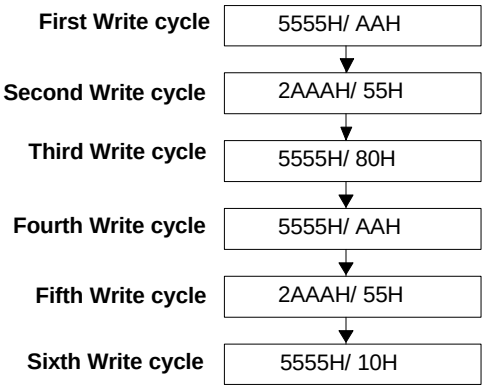


Figure 3. Embedded Programming Algorithm

Note: See Data Polling Algorithm in Figure 5

Chip Erase Command Sequence (Address/Data)



Individual Sector/Multiple Sector Erase Command Sequence (Address/Data)

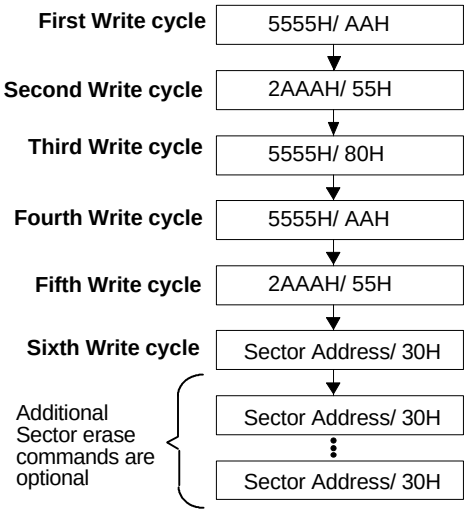
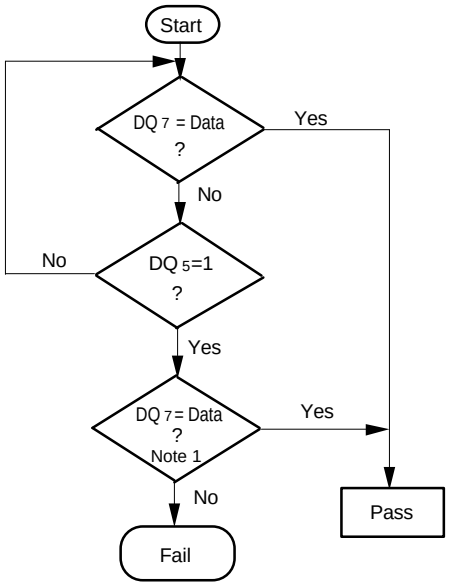


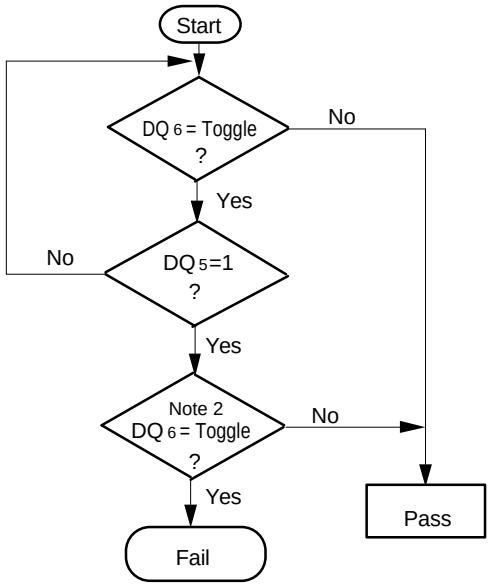
Figure 4. Automated Erase Flow Chart and Sequence

Data Polling Algorithm



Note: DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Toggle Bit Algorithm



Note: DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 is changed to "1".

Figure 5. Data Polling and Toggle Bit Algorithm

Absolute Maximum Ratings:

Storage Temperature	-65°C to +125°C
Operating Temperature (Note 1)	
During Read	-55°C to +125°C
During Program/Erase	-55°C to +125°C
Temperature under Bias (With Power Applied)	-55°C to +125°C
Voltages with Respect to GND.	
All pins except A9 (Note 2, 3)	-2V to +7V
Vcc (Note 2)	-2V to +7V
A9 (Note 3)	-2V to +14V
Output short circuit current (Note 4)	200 mA

Operating Ranges:

Commercial (C) Devices

Temperature Range	0°C to +70°C
Vcc supply voltage during all operations	4.5V to 5.5V or 4.75V to 5.25V

Industrial (I) Devices

Temperature Range	-40°C to +85°C
Vcc supply voltage during all operations	4.5V to 5.5V

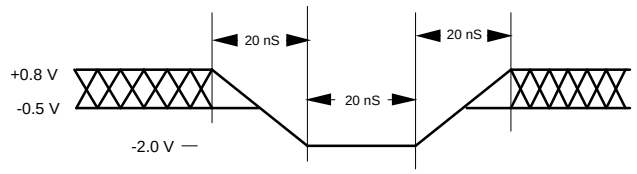
Notes :

1. The datasheet defines the operation at specific temperature ranges.
2. Minimum DC voltage on input / output pins is -0.5V. During voltage transitions, inputs can undershoot to -2 Volts for periods of up to 20 nS. The maximum DC voltage on these pins is Vcc +0.5V. During transitions, inputs may overshoot to Vcc +2.0V for periods < 20 nS.
3. Maximum DC voltage on A9 may overshoot to 14.0V for periods < 20 nS.
4. Outputs may be shorted for no more than one second. Only one/output can be shorted at a time.

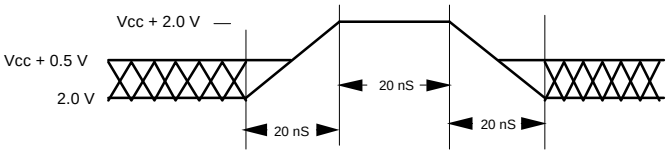
**Notice: Stresses above those listed under "Absolute Maximum Ratingsz" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*

Maximum Overshoot

Maximum Negative Overshoot



Maximum Negative Overshoot Waveform



Maximum positive Overshoot Waveform

Figure 6. Maximum Overshoot Waveforms

DC Characteristics

PARAMETER	SYM.	MIN.	MAX.	UNIT	TEST CONDITIONS
Input Low Level	V_{IL}	-0.5	0.8	V	
Input High Level	V_{IH}	2.0	Vcc +0.5	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 12 mA Vcc = Vcc Min.
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -2.5 mA Vcc = Vcc Min.
Output High Voltage	V_{OH2}	Vcc -0.4		V	I_{OH}I = -100 µA Vcc = Vcc Min.
Input Load Current	I_{LI}		+/- 1.0	µA	Vin = Vcc or GND Vcc = Vcc Max.
Output Leakage Current	I_{LO}		+/- 10	µA	Vout = Vcc or GND Vcc = Vcc Max.
Output Short Circuit Current	I_{OS}		100	mA	Vout = 0.5V, Vcc = Vcc Max.
Vcc Standby Current (CMOS) 4	I_{SB1}		100	µA	$\overline{CE}$ = Vcc +/- 0.5V, Vcc = Vcc Max.
Vcc Standby Current (TTL) 4	I_{SB2}		1.0	mA	$\overline{CE}$ = V_{IH} Vcc = Vcc Max.
Vcc Active Current Read 1, 3	I_{CC1}		40	mA	$\overline{CE}$ = V_{IL}, f = 6 MHz, $\overline{CE}$ = V_{IH}
Vcc Active Current Program or 2	I_{CC2}		60	mA	$\overline{CE}$ = V_{IL}, $\overline{CE}$ = V_{IH}
A9 Intelligent Identifier Volatge	V_{ID}	11.5	12.5	V	
A9 Intelligent Identifier Current	I_{ID}		50	µA	A9 = V_{ID}

Table 9

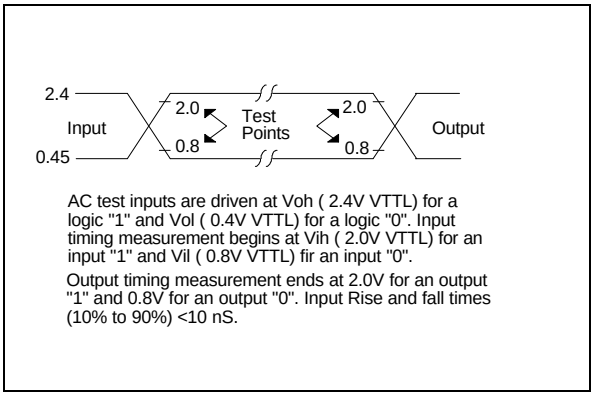
Notes:
1. All Currents are in RMS unless otherwise noted. Typical values are Vcc = +5.0V, T = 25° C.
2. These parameters are sampled but not 100% tested.
3. Automatic power saving reduces the Iccr to 1 mA.
4. CMOS inputs are Vcc +0.5V. TTL inputs are either V_{IL} or V_{IH}.

Capacitance:

T_A = 25° C, f = 1 MHZ (2)

PARAMETER	SYMBOL	CONDITIONTION	TYPICAL	MAX.	UNIT
Input Capacitance	Cin	Vin = 0V	6	8	pF
Output Capacitance	Cout	Vout = 0V	10	12	pF

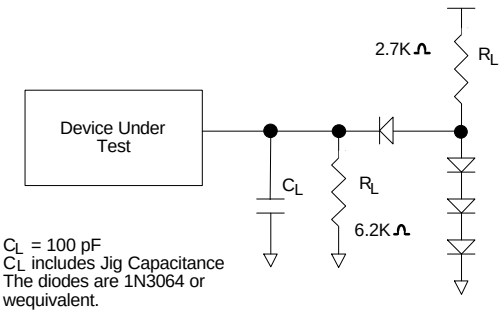
AC Testing Input/Output Waveform



AC test inputs are driven at Voh (2.4V VTTL) for a logic "1" and Vol (0.4V VTTL) for a logic "0". Input timing measurement begins at Vih (2.0V VTTL) for an input "1" and Vil (0.8V VTTL) fir an input "0".

Output timing measurement ends at 2.0V for an output "1" and 0.8V for an output "0". Input Rise and fall times (10% to 90%) <10 nS.

AC Testing Load Circuit



C_L = 100 pF
C_L includes Jig Capacitance
The diodes are 1N3064 or wequivalent.

Figure 7. A.C.Testing Load and Waveforms

AC Characteristics - Read Only Operations (1)

SYMBOL (4)		DESCRIPTION	-75	-90	-120	-150	UNITS
JEDEC	Standard						
tAVAV	tRC	Read Cycle Time	70	90	120	150	nS
tAVQV	tACC	Address to Output Delay	70	90	120	150	nS
tELQV	tCE	$\overline{CE}$ low to Output Delay (2)	70	90	120	150	nS
tGLQV	tOE	$\overline{OE}$ low to Output Delay	30	35	50	55	nS
tELQX	tLZ	$\overline{CE}$ low to Output LOW Z (3)	0	0	0	0	nS
tEHQZ	tHZ	$\overline{CE}$ high to Output HIGH Z	20	20	30	35	nS
tGLQX	tOLZ	$\overline{OE}$ low to Output LOW Z	0	0	0	0	nS
tGHQZ	tDF	$\overline{OE}$ high to Output HIGH Z (3)	20	20	30	35	nS
tAXQX	tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever is first (1)	0	0	0	0	nS

Table 11

Notes:
1. See A.C. Input/Output Reference Waveforms for timing measurements.
2. $\overline{OE}$ may be delayed up to tCE-tOE after the falling edge of $\overline{CE}$ without impact on tCE.
3. Sampled, not 100% tested.
4. See A.C. Input/Output Reference Waveforms and A.C. Testing Load Circuits for testing characteristics.

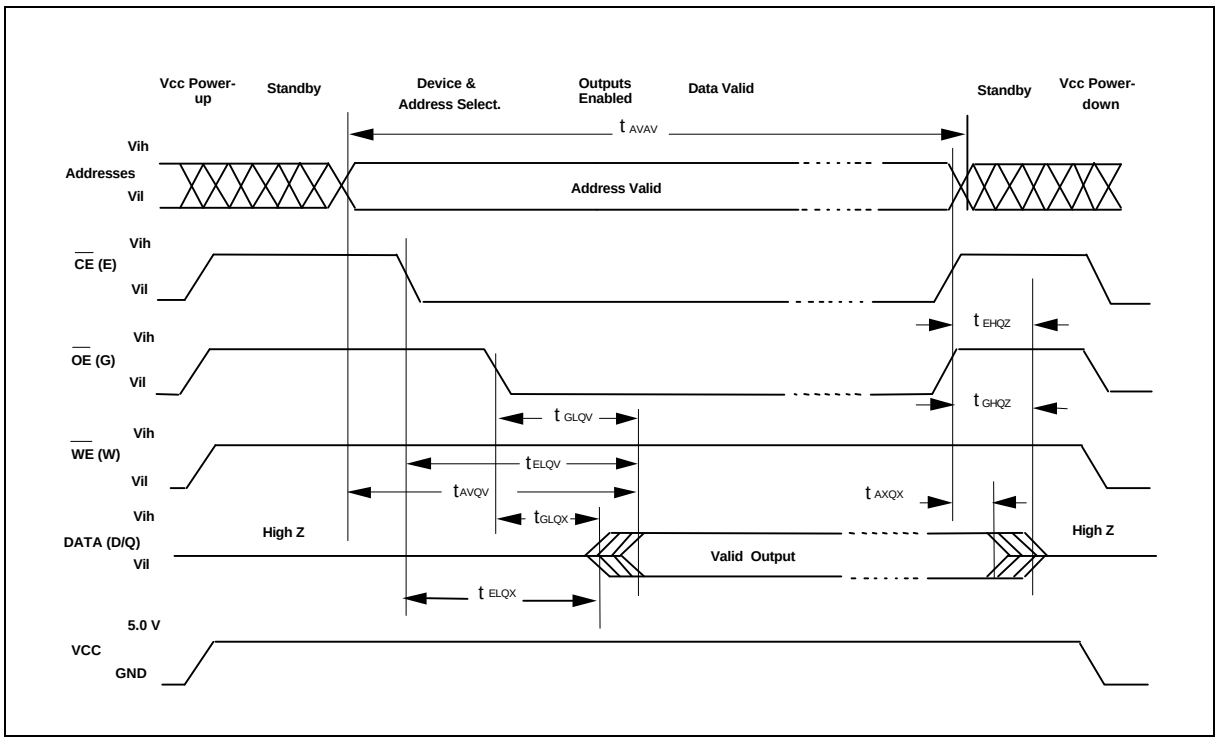


Figure 8. A.C.Waveforms for Read Operations

AC CHARACTERISTICS - for $\overline{WE}$ Controlled Write Operation

SYMBOL		DESCRIPTION		-75	-90	-120	-150	UNITS
JEDEC	Standard							
tAVAV	tWC	Write Cycle Time (4)		70	90	120	150	nS
tELWL	tCS	$\overline{CE}$ Setup		0	0	0	0	nS
tAVWL	tAS	Address Setup Time		0	0	0	0	nS
tDVWH	tDS	Data Setup Time		30	45	50	55	nS
tWLWH	tDH	Data Hold Time		0	0	0	0	nS
tWHEH	tCH	$\overline{CE}$ Hold Time		0	0	0	0	nS
tWLAX	tAH	Address Hold Time		45	45	50	50	nS
tWLWH	tWP	Write Pulase Width		35	45	50	50	nS
tWHWL	tWPH	$\overline{WE}$ Pulse Width High		20	20	20	25	nS
	tOES	Output Enable Setup Time		0	0	0	0	nS
	tOEH	Output Enable Hold Time	Read (4)	0	0	0	0	nS
			Toggle and Data Polling	10	10	10	10	nS
tGHWL	tGHWL	Read Recover Time Before Write		0	0	0	0	nS
tWHWH1	tWHWH1	Programming Operation		16	16	16	16	µS
tWHWH2	tWHWH2	Erase Operation (min.) (1)	typ	1.5	1.5	1.5	1.5	sec
			max	30	30	30	30	sec
	tVCS	Vcc Setup Time	(4)	50	50	50	50	µS
	tVLHT	Voltage Transition Time	(2, 4)	4	4	4	4	µS
	tWPP1	Write Pulse Width	(2)	100	100	100	100	µS
	tWPP2	Write Pulse Width	(2)	10	10	10	10	mS
	tCESP	$\overline{CE}$ Setup Time to $\overline{WE}$ Active	(3, 4)	4	4	4	4	µS
	tOESP			4	4	4	4	µS

Table 12

Notes:
1. The Erase operation does not need programming time.
2. These timings are for Sector Protect/Unprotect operation.
3. This timing is only for sector Unprotect.
4. Not 100% tested.

Switching Waveforms

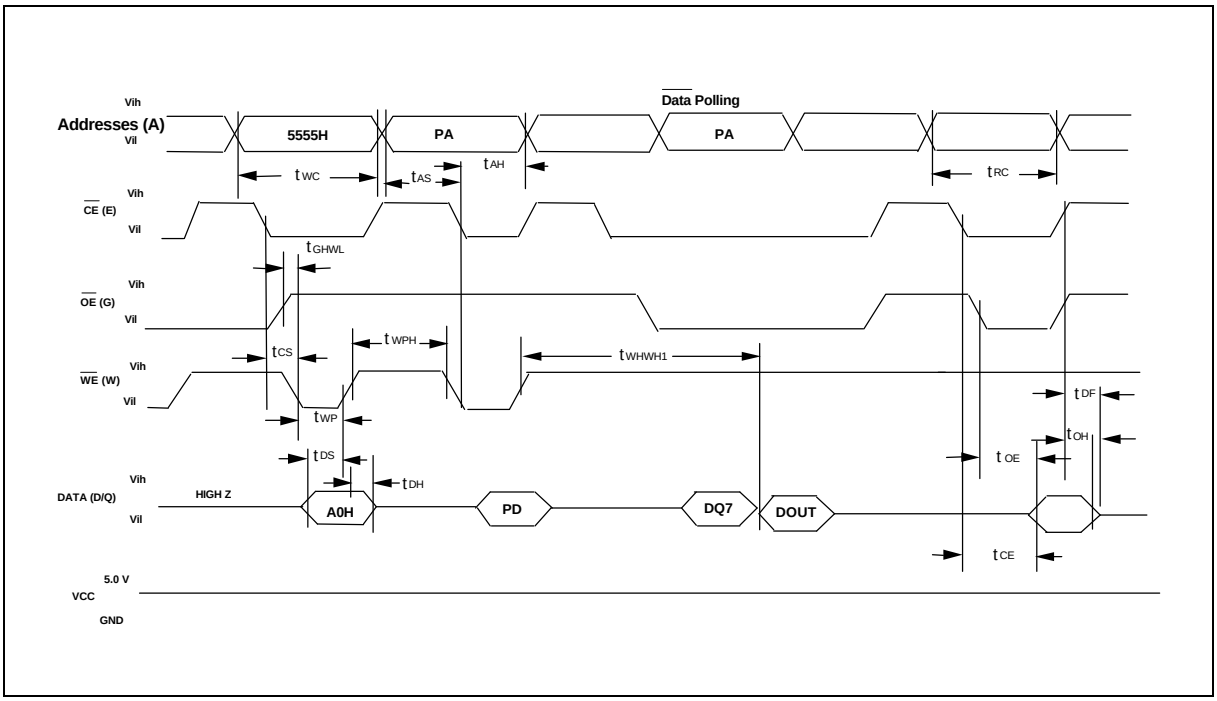


Figure 9. A.C.Waveforms for Program Operations ($\overline{WE}$ Controlled Writes)

Notes:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at the byte address.
3. DQ7 is the output of the complement of the data written tot he device.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of four bus cycle sequence.

AC CHARACTERISTICS - for $\overline{CE}$ Controlled Write Operation

SYMBOL		DESCRIPTION		-75	-90	-120	-150	UNITS
JEDEC	Standard							
tAVAV	tWC	Write Cycle Time (Note 4)		70	90	120	150	nS
tWLEL	tWS	$\overline{WE}$ Setup time		0	0	0	0	nS
tAVEL	tAS	Address Setup time		0	0	0	0	nS
tDVEH	tDS	Data Setup time		30	45	50	50	nS
tEHDX	tDH	Data Hold time		0	0	0	0	nS
tEHWH	tWH	$\overline{WE}$ Hold time		0	0	0	0	nS
tWLAX	tAH	Address Hold time		45	45	50	50	nS
tELEH	tCP	$\overline{CE}$ Pulse Width		35	45	50	50	nS
tEHEL	tCPH	$\overline{CE}$ Pulse Width High		20	20	20	25	nS
	tOES	Output Enable Setup time		0	0	0	0	nS
	tOEH	Output Enable Hold time	Read (Note 4)	0	0	0	0	nS
			Toggle and Data Polling	10	10	10	10	nS
tGHEL	tGHEL	Read Recover time before Write		0	0	0	0	nS
tWHWH1	tWHWH1	Programming Operation		16	16	16	16	uS
tWHWH2	tWHWH2	Erase Operation (1)	typ	1.5	1.5	1.5	1.5	sec
			max	30	30	30	30	sec
	tVCS	Vcc Setup time (Note 4)		50	50	50	50	µS

Table 13

Notes:

1. The Erase operation does not need programming time.

2. These timings are for Sector Protect/Unprotect operation.

3. This timing is only for sector Unprotect.

3. Not 100% tested.

Switching Waveforms

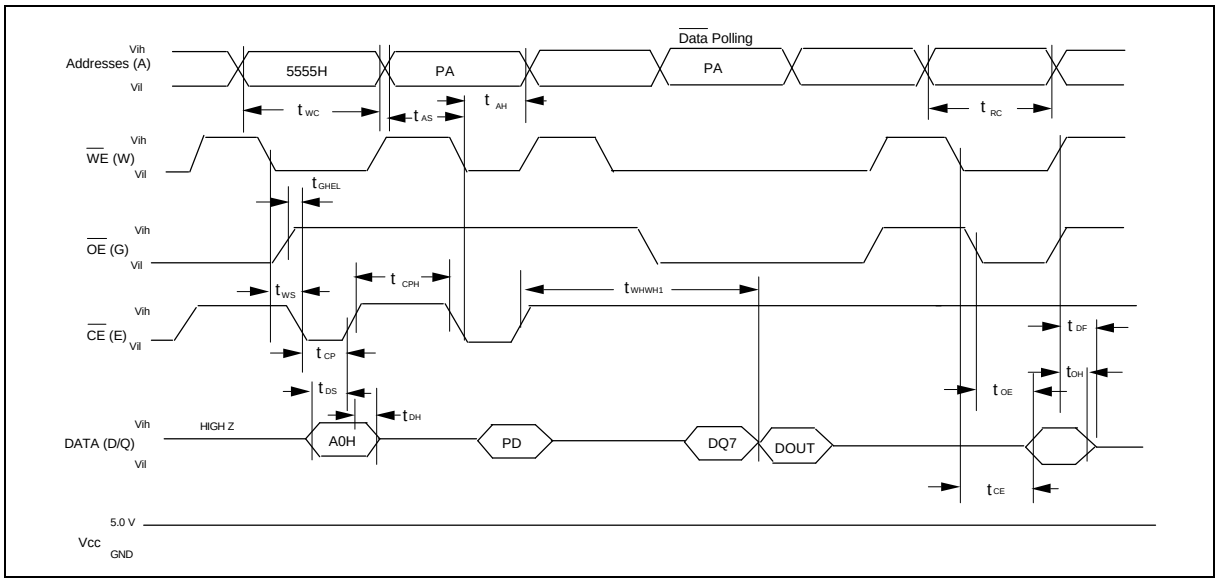


Figure 10.A.C.Waveforms for Program Operations ($\overline{CE}$ Controlled Writes)

Notes:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at the byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Switching Waveforms

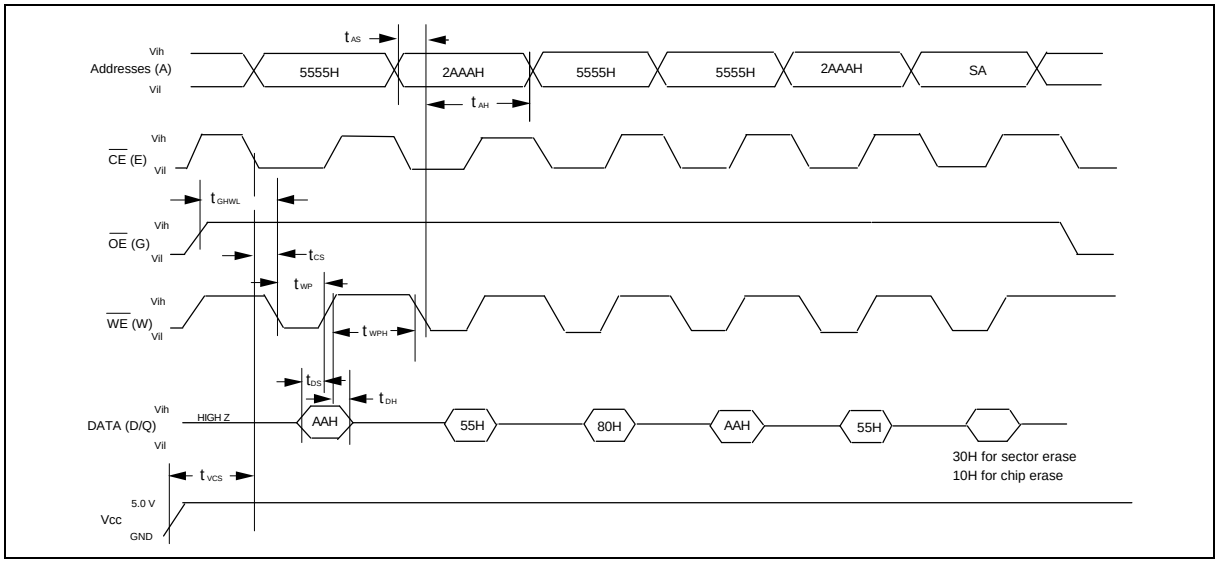


Figure 11. A.C. Waveforms for Chip/Sector Erase Operations

Note: SA is the sector address for Sector erase or 5555H for Chip Erase.

Switching Waveforms

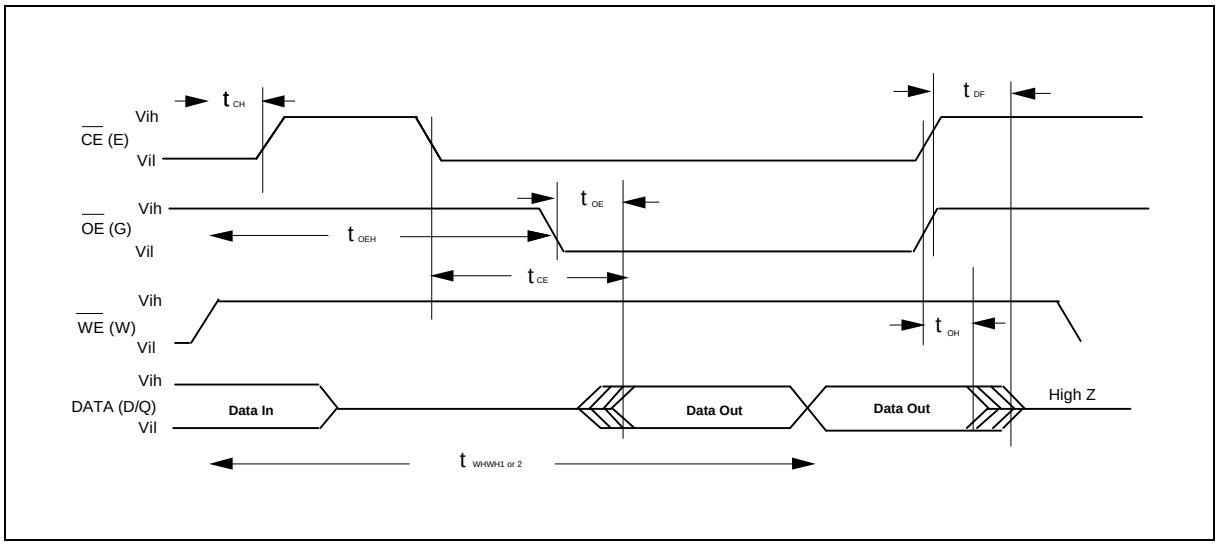


Figure 12. AC Waveforms for Data Polling during Embedded Algorithm operations

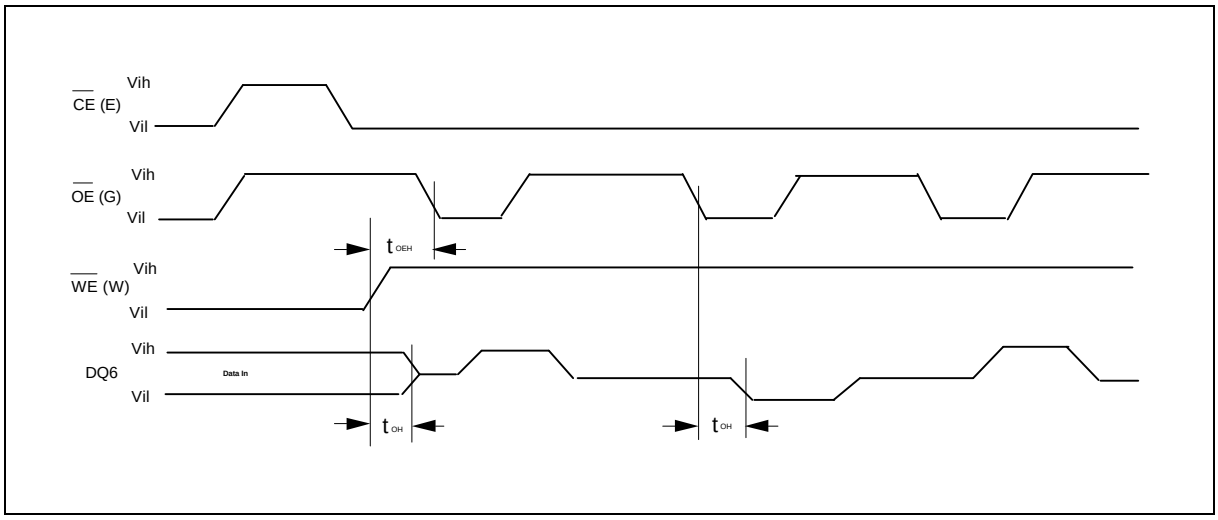


Figure 13. AC Waveforms for Toggle Bit during Embedded Algorithm operations Operating

ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	PACKAGE	CYCLING (Min)	TEMPERATURE RANGE
29F040-90NC	90	60	32 PDIP	10,000	0°C - 70°C
29F040-12NC	120	60	32 PDIP	10,000	0°C - 70°C
29F040-90AC	90	60	32 PLCC	10,000	0°C - 70°C
29F040-12AC	120	60	32 PLCC	10,000	0°C - 70°C
29F040-90TC	90	60	32 TSOP	10,000	0°C - 70°C
29F040-12TC	120	60	32 TSOP	10,000	0°C - 70°C
29F040-90NI	90	60	32 PDIP	10,000	-40°C - 85°C
29F040-12NI	120	60	32 PDIP	10,000	-40°C - 85°C
29F040-90AI	90	60	32 PLCC	10,000	-40°C - 85°C
29F040-12AI	120	60	32 PLCC	10,000	-40°C - 85°C
29F040-90TI	90	60	32 TSOP	10,000	-40°C - 85°C
29F040-12TI	120	60	32 TSOP	10,000	-40°C - 85°C

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.
3. Typical cycling is 100,000 program and erase cycles.

APPENDIX A

Compatibility to AMD's AMD29F040B

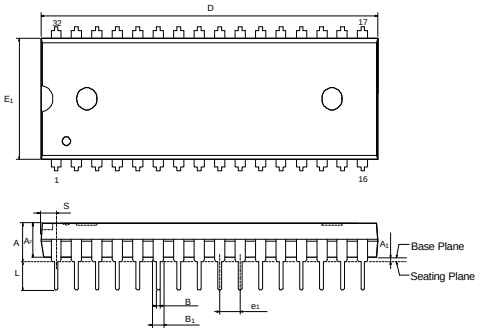
The device is fully functional compatible to the AMD29F040B except during the command addresses subset mode. In the AMD device, Commands do not require a unique address pattern for bits A15, A14, A13, A12 or A11 (eg.X555H or X2AAH instead of 5555H and 2AAAH). That is, the BM29F040 requires specifically A14,A13,A12 and A11 to be forced during the command sequence in addition to A10 through A0. Note specifically that the BM29F040 does not require address A15 along with A18, A17 and A16 to be forced during the command sequence.

AMD's reduced address requirement makes their device slightly easier to inadvertently create a Command and cause some program error or malfunction. The advantage of reducing the address is to simplify the hardware interface in systems where control signals are limited in number. The 29F040B reduces the interface requirement by 4 signals -- from 15 to 11 address control pins.

However if the full Command address is supplied (i.e. 2AAAH and 5555H) by the host system, there will be no incompatibility using either device.

PACKAGE DIMENSIONS

32-pin P-DIP

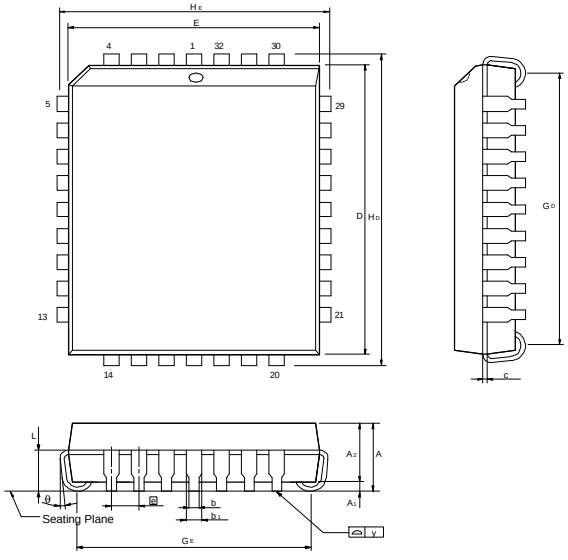


Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches
6. General appearance spec. should be based on final visual inspection spec.

32-pin PLCC



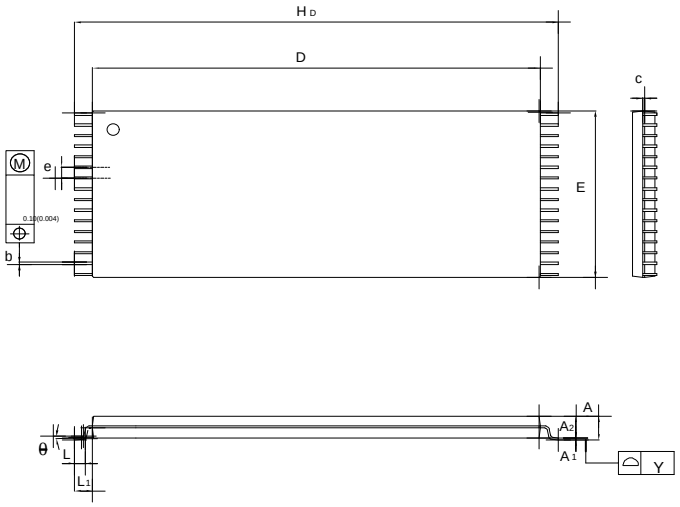
Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.51	0.530	12.45	12.9	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.49	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection sepc.

Package Dimensions, continued

32-pin TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Note:
Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jun. 1999	-	Initial Issued

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