XRT95L51

OC-48 ATM UNI/POS/MAPPER IC

JULY 2000 REV. P1.0.1

GENERAL DESCRIPTION

The XRT95L51 is an ATM/PPP physical layer processor with integrated SONET OC-48/STM-16 framing controller. ATM direct mapping and cell delineation are supported, as are PPP mapping and frame processing. The XRT95L51 contains an integral SONET framer which provides framing and error accumulation in accordance with ANSI/ITU-T specifications. The configuration of this device is done through internal registers accessible via 8-bit parallel, memory mapped, microprocessor interface.

The XRT95L51 provides full section, line and path overhead processing and supports scrambling/descrambling, alarm signal insertion/detection and bit interleaved parity processing.

The SONET/SDH transmit and receive blocks are used to transmit/receive an OC-48c/STM-16c signal or compose and decompose four OC-12/12c signals.The blocks operate at a peak internal clock speed of 77 MHz and support 32-bit internal data paths. The transmit and receive blocks are compliant with both SONET and SDH standards.

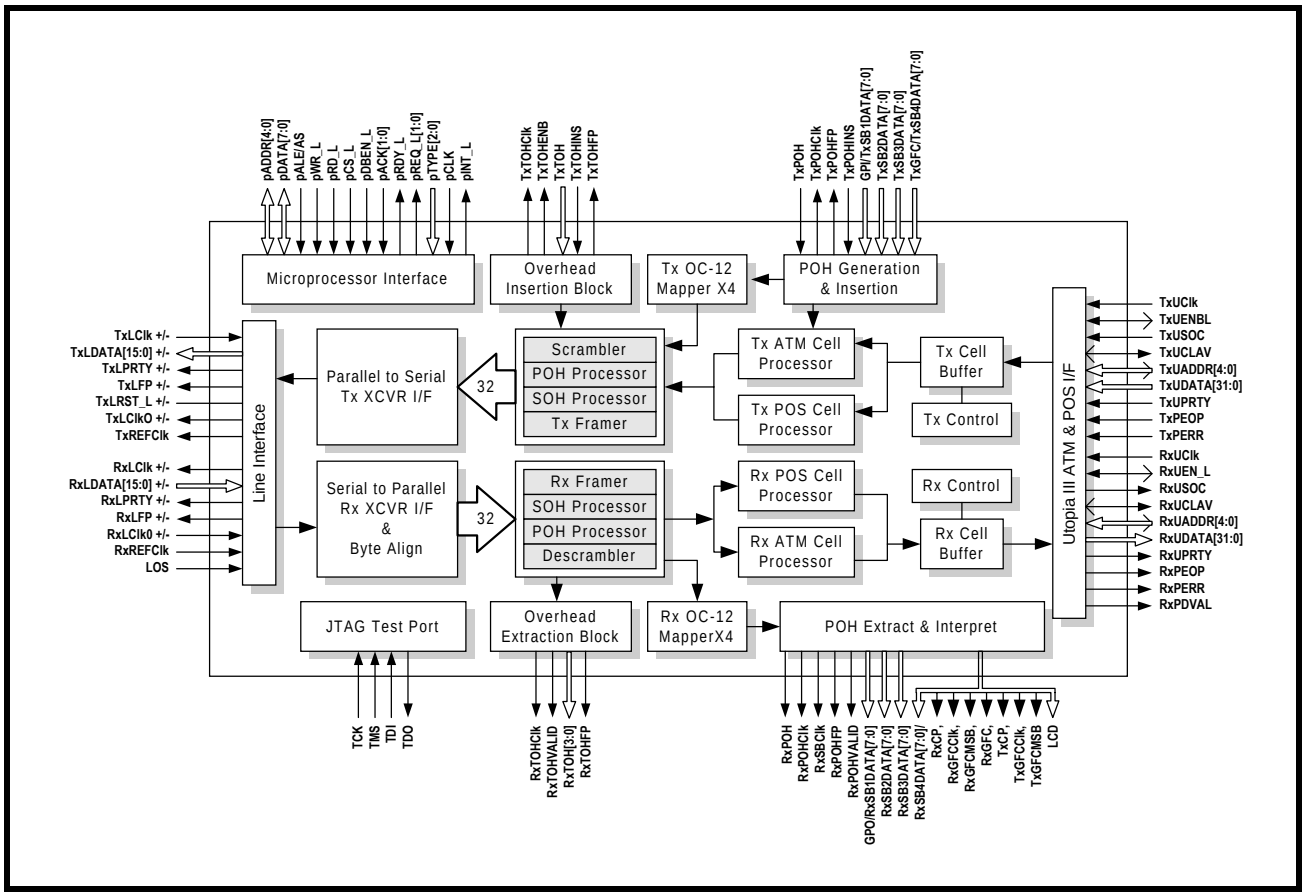
APPLICATIONS

- Digital Cross Connect Systems
- ATM Switches
- Routers
- SONET/SDH Add Drop Multiplexers
- Multiplexers

FEATURES

- Single chip for ATM UNI and Packet over SONET.
- Generates and terminates SONET section, line and path layers.
- Provides SONET frame scrambling and descrambling.
- Provides 32-bit data UTOPIA level II and III multi-PHY interface and POS-PHY interface.
- 8-bit microprocessor interface
- Includes ATM cell or PPP packet mapping
- Single +3.3V power supply with +5V input tolerance
- -40°C to +85°C Operating Temperature Range
- Available in a 388 pin PBGA package

FIGURE 1. BLOCK DIAGRAM OF THE 95L51 OC-48 ATM UNI/POS/MAPPER IC



FUNCTIONAL OVERVIEW

XRT95L51 implements the SONET/SDH framing function with full duplex ATM/POS interface for the STS-48/STM-16 data streams.The XRT95L51 is functionally and architecturally, divided into the following blocks and modules:

LINE SIDE INTERFACE

- Differential inputs/outputs for high speed chip-to-chip communication using Pseudo ECL logic.
- Programmable parity bit for both incoming and outgoing data paths.
- Monitors the Loss of Optical Carrier.
- The transmit line side provides the direct looped back version of the line clock, framing pulse and parity.
- The reference signal derived from the receive clock input can be programmed to be 77.76 MHz,38.88 MHz,19.44 MHz or 8 kHz.
- The reference signal derived from the transmit clock input can be programmed to be 77.76 MHz,38.88 MHz, 19.44 MHz and 8 kHz.
- 8 kHz reference signal can be phase locked to either incoming or outgoing SONET/SDH frame.
- Supports Local and Remote Line Loopback.
- Provides 155.52 MHz 16-bit parallel interface

SONET/SDH TRANSMITTER

- Performs standard OC-48c/STM-16c transmit processing
- Conforms to IYU-T I.432,ANSI.105 and Bellcore GR-253
- Performs SONET/SDH frame insertion and accepts external frame synchronization
- Performs optional transmit data scrambling
- Performs POH,TOH generation/insertion
- Generates transmit payload pointer (H1,H2) (fixed at 522) with NDF insertion
- Inserts A1/A2 with optional error mask
- Computes and inserts BIP-8 (B1,B2) with optional error mask
- Generates AIS-L,REI-L and RDI-L according to receiver state with option of SW/HW insertion
- Inserts LOS, forces SEF by software
- Generates RDI-P and REI-P automatically with optional SW/HW override
- Inserts fixed stuff columns, calculates and inserts B3 error code
- Performs payload insertion from cell processor

SONET/SDH RECEIVER

- Performs standard STS-48c/STM-16c receive processing
- Provides fully programmable threshold detection for SD and SF condition
- Provides 155.52MHz 16-bit parallel interface
- Provides section trace buffer with mis-match detection and invalid message detection
- Performs SONET/SDH frame synchronization
- Supports NDF, positive stuff and negative stuff pointer processor
- Performs receive data de-scrambling
- Performs POH,TOH interpretation/extraction
- Interprets payload pointer (H1,H2)
- Extracts data communication channels from D1-D3 and D4-D12
- Detects out of frame (OOF), loss of frame (LOF), loss of signal (LOS), APS failure
- Detects Line Alarm Indication (L-AIS), Line remote Defect Indication (L-RDI), Loss of Pointer
- Detects Path Alarm Indication, Path remote Defect Indication, Path extended RDI
- Provides signal label monitor with PLM detection
- Supports path travel buffer with TIM-P and invalid message detection
- Computes and compare B3,REI-L and REI-P errors
- Computes and compare BIP-8 (B1,B2) and counts the errors
- Performs payload extraction.

ATM CELL PROCESSOR

- Implements the ATM physical layer for Broadband ISDN according to ITU-T Recommendation I.432
- Supports SDH mapping
- Provides selectable on-going HEC insertion and verification
- Provides selectable Coset addition and removal
- Provides single bit error correction and multiple bit error detection for HEC processing
- Provides HEC correctable and uncorrectable indications
- Provides HEC correction selectability
- Supports external cell GFC insertion and extraction
- Provides the functions of cell rate de-coupling; idle cell insertion and detection, 16-cell FIFO cell buffering, programmable idle cell header and payload and idle cell HEC generation

- Offers cell delineation with three states (hunt, pre-sync and sync) synchronization algorithm and provides LCD (Loss of Cell Delineation) indication and interrupt
- Supports multiple programmable VPI/VCI filters on Transmit and Receive
- Provides self-synchronizing SDH cell scrambling/ de-scrambling, $x^{43}+1$
- Supports OAM cell insertion and extraction with dedicated cell store via microprocessor interface. Transmission is enabled through semaphore
- Provides TXCell and TXCell indication signals
- Provides test cell generation and verification

PACKET OVER SONET (POS) PROCESSOR

- Supports packet based link protocols by using byte synchronous HDLC framing like PPP,HDLC and frame relay
- 32-bit extended Saturn POS-PHY host interface clocked to 100 MHz
- Performs transmit HDLC frame insertion and receive data extraction
- Performs self-synchronous data scrambling and de-scrambling using$1+X^{43}$ polynomial
- Performs transmit flag sequence insertion and receive synchronization
- Performs byte stuffing and de-stuffing for transparency processing
- Performs optional CRC-CCITT and CRC-32 FCS generation and error checking
- Supports optionally flow-through mode
- Performs abort sequence insertion and detection
- Arbitrary packet length (1 or more octets) and flag sharing (single flag between frames)
- Provide minimum and maximum packet length checking, removing and reporting
- Transparency by octet stuffing of flag (0x7E), control escape (0x7D) and abort sequence
- Automatic transfer halt on receive FIFO host-side at end of packet
- Error detection for Underflow of transmit FIFO, Overflow of receive FIFO, parity error on transmit
- Optional removal of FCS from receive frames
- Optional transmit FCS insertion

UTOPIA / POS-PHY INTERFACE

- Complies with ATM forum Utopia Level 2 and 3 Specification
- Supports 32-bit 100MHz Transmit and Receive interface
- Provides up to total 16 cell buffers for transmit and receive
- Transmits and receives both 52 and 54 byte cell
- Generates and checks data parity of Utopia interface
- Supports programmable Transmit CLAV (transmit cell available) signal for 0,1,2,3 cell look ahead
- Supports programmable Receive CLAV (receive cell available) signal for 0,1,2,3 byte look ahead
- Provides 32-bit up to 100 MHz industrial standard POS-PHY interface

PERFORMANCE MONITORING

- Supports line path performance monitoring
- Provides 32-bit saturating counter of idle cells transmitted
- Provides 32-bit saturating counter of assigned cells transmitted
- Provides 32-bit saturating counter of valid cells received
- Provides 32-bit saturating counter of idle cells received
- Provides 32-bit saturating counter of cells received with HEC error
- Provides 32-bit saturating counter of cells discarded
- Provides 32-bit saturating counter of REI-L errors
- Provides 32-bit saturating counter of REI-P errors
- Provides 32-bit saturating counter of BIP-8 (B1,B2 and B3) errors
- Provides 32-bit saturating counter of POS frame check sequence errors
- Provides 32-bit saturating PPP good frame counter
- Provides 32-bit saturating PPP bad FCS counter
- Provides 32-bit saturating PPP aborted frame counter
- Provides 32-bit saturating PPP Runt frame counter

INTERRUPT, STATUS AND TEST

- Provides individually maskable interrupts
- Provides one second interrupt generations
- Generates interrupts from the following causes: OOF status change, LOS status change, AIS status change, COFA, Utopia/PPP-PHY parity error, Utopia/PPP-PHY FIFO overrun, Utopia/PPP-PHY FIFO under-run, change of cell alignment, HEC errors, LCD status change
- Provides Local and Remote Line Loopback
- Provides SONET Remote Loopback
- Provides local ATM/PPP and UTOPIA Loopback
- Supports IEEE 1149.1 JTAG testing

FIGURE 2. TYPICAL APPLICATION

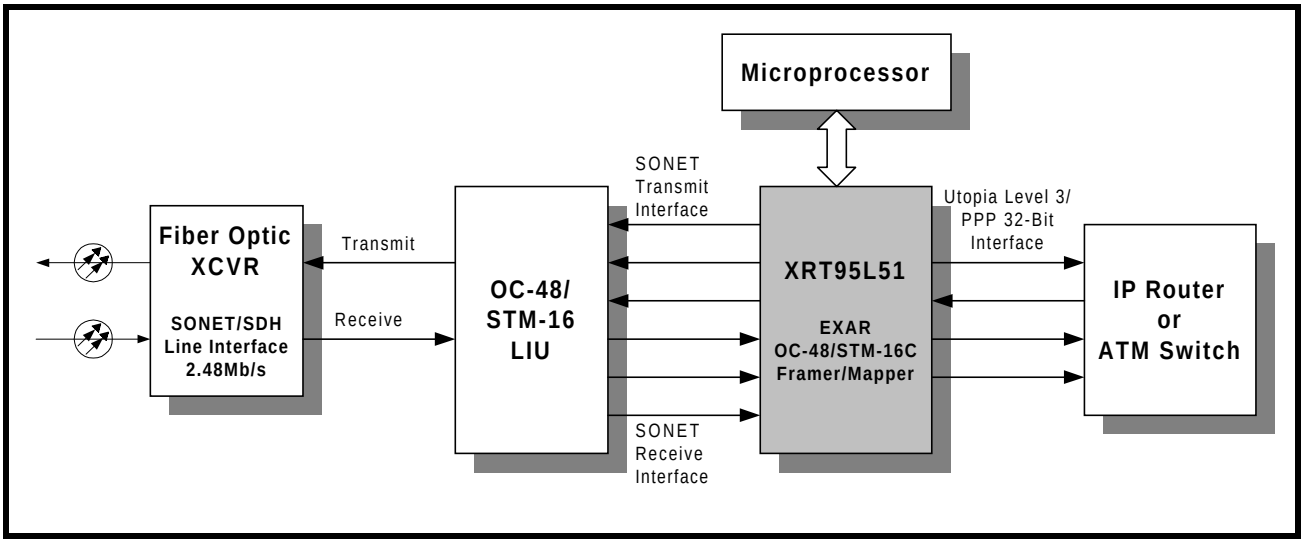


FIGURE 3. PIN OUT OF THE XRT95L51 IN THE 388 PIN PBGA PACKAGE

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GNDAP	VCCAP	TADDR6	TADDR2	TREFPLL	TXREF CLK	GP14	GP11	TXSB2 D2	TXSB2 D2	TXTOH CLK	TXSB3 D2	TXSB3 D1	TXSDCC	TXE1F1 E2FP	TXSB4 D3	TXSB3 D4	TXSB3 D1	TXGFC	TXSB4D4	TXSB3 D5	TXUD8	TXUD18	TXUD5	TDMUXE N1	GNDAP	A
B	nc	TXLCLKP	TADDR9	TADDR5	TADDR1	TXSBCLK	GP16	GP10	TXSB2D6	TXSB3D3	TXTOH ENB	TXSB3D7	TXTOH	TXLDCC ENB	TXSB3 D6	TXE1F1	TXSB4 D2	TXSB4 D7	TXSB3 D6	TXUD15	TXUD9	TXU10	TXUD6	TDMUX EN2	TWEN	VCCAP	B
C	TXLRST LP	TXLCLK OP	TXLCLKN	TADDR8	TADDR4	TADDR0	NC	GP15	TXSB2 D7	TXSB2 D4	TXSB2 D0	TXTOHFP	TXSDCC ENB	TXE1F1E2 ENB	TXSB3 D5	TXPOH CLK	TXPOH INS	TXPOH	TXUD13	TXUD16	TXUD17	TXUD19	TXUCLK	TREN	NC	TXUD20	C
D	TXL PRTYP	TXLRST _LN	TXLCLK ON	nc	TADDR7	TADDR3	TPPLL	GP17	GP13	GP12	TXSB2 D1	TXSB2 D3	TXTOH INS	TXLDCC	TXSB3 D0	TXPOH ENB	TXPOHFP	TXUD14	TXUD12	TXUD11	TXUD7	TXUD CLK0	TDMUX EN0	NC	TXUD4	TXUSOC	D
E	TXLD15N	TXLRST PRTYN	TXLFPP	nc																			TXUD27	TXUEN_L	TXUD28	TXUD3	E
F	TXLD14N	TXLD6N	TXLD15P	TXLFPN																			TXUCLAV	TXUD26	TXUPRTY	TXUA0	F
G	TXLD13P	TXLD5N	TXLD14P	TXLD6P																			TXUD21	TXUA4	TXUD2	TXUD1	G
H	TXLD4P	TXLD12P	TXLD13N	TXLD5P																			TXUD29	TXPEOP	TXUD22	TXUA3	H
J	TXLD11N	TXLD11P	TXLD4N	TXLD12N																			TXUD25	TXUD30	TXUA1	TXUD0	J
K	TXLD10N	TXLD10P	TXLD3N	TXLD3P																			TXUD24	TXPERR	TXUA23	TXUA2	K
L	TXLD2N	TXLD9P	TXLD9N	TXLD2P							V3	V3	V3	V3	V3	V3							TXUD31	NC	NC	RXUD9	L
M	TXLD8N	TXLD8P	TXLD1N	TXLD1P							V1	V1	G	G	V2	V2							RXUD10	RXUD8	RXUD13	RXUD12	M
N	TXLD0N	TXLD7P	TXLD7N	TXLD0P							V1	V1	G	G	V2	V2							RXUD11	RXUA3	RXUA4	RXUSOC	N
P	RXLD15P	RXLD15N	RXLD0PN	RXLD0N							V1	V1	G	G	V2	V2							RXUCLAV	RXUD7	RXUD14	RXUD26	P
R	RXLD14P	RXLD14N	RXLD1N	RXLD1P							V1	V1	G	G	V2	V2							RXUD15	RXUEN_L	RXUD27	RXUD25	R
T	RXLD13P	RXLD13N	RXLD2P	RXLD12P							G	G	G	G	G	G							RXUA2	RXUD24	RXUD6	RXUD16	T
U	RXLD3P	RXLD3N	RXLD2N	RXLD11P																			RXUD5	NC	RXUD28	RXPDVAL	U
V	RXLD12N	RXLD11P	RXLD4P	RXLD4N																			RXUD17	RXUD23	RXUA1	RXUD18	V
W	RXLD10N	RXLD10P	RXLD9N	RXLD5N																			RXUA0	RXUD19	RXU D29	RXPERR	W
Y	RXLD9P	RXLD5P	RXLD8N	RXLD7P																			RXUD20	NC	RXUD 22	RXP EOP	Y
AA	RXLD8P	RXLD6P	RXLD7N	RXLFPP																			RXUD2	RXUD31	RXUPRTY	RXUD30	AA
AB	RXLD6N	RXL PRYTP	RXLFPN	RXL CLKN																			RXUDCL K	RXUD0	RXUD3	RXUD21	AB
AC	RXLPRTY N	NC	NC	GNDAP	RXLDCC VAL	LOF	RXPOH CLK	RXTOH	RXTOH VAL	PREQ_L1	PADDR3	RXSB2D3	RXSB2D2	PDATA6	RXSB2D0	PALE	PDATA4	PCS_L	PDATA3	TXGFC CLK	TXGFC MSB	LCD	TMS	TRST_L	RXUCLK0	RXUD1	AC
AD	RXLCLKP	RXL CLKOP	VCCAP	RXSDCC	RXPOHFP	LOS	RESET_L	RXTOHFP	PADDR4	GPO4	PINT_L	PDATA7	PWR_L	PADDR1	PADDR0	PTYPE2	PCLK	RXSB3D5	RXSB3D4	PRDY_L	PDATA2	PBLAST_ L	RXE1F1 E2FP	TCK	TDO	NC	AD
AE	RXL CLKON	RXREF CLK	RXSD CCVAL	LOPC	RXPOH VAL	RXPOH	TEST MODE	GPO2	GPO5	GPO0	PREQ_L0	PADDR2	PACK_L1	RXSB2D1	RXSB2D4	RXSB2D3	RXSB3D2	RXSB3D1	PTYPE1	PTYPE0	PDATA0	PDBEN_L	RXE1F1 E2VAL	RXE1 F1E2	RXGFC	TDI	AE
AF	NC	RXSBCLK	RXLDCC	SEF	NC	GPO7	GPO3	GPO6	GPO1	RXTOH CLK	RXSB2D7	RXSB2D6	RXSB2D5	PACK_L0	PRD_L	PDATA5	RXSB3D7	RXSB3D6	PDATA1	RXSB3D0	TXCP	RXCP	RXGFC CLK	RXGFC MSB	VCCAP	GNDAP	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

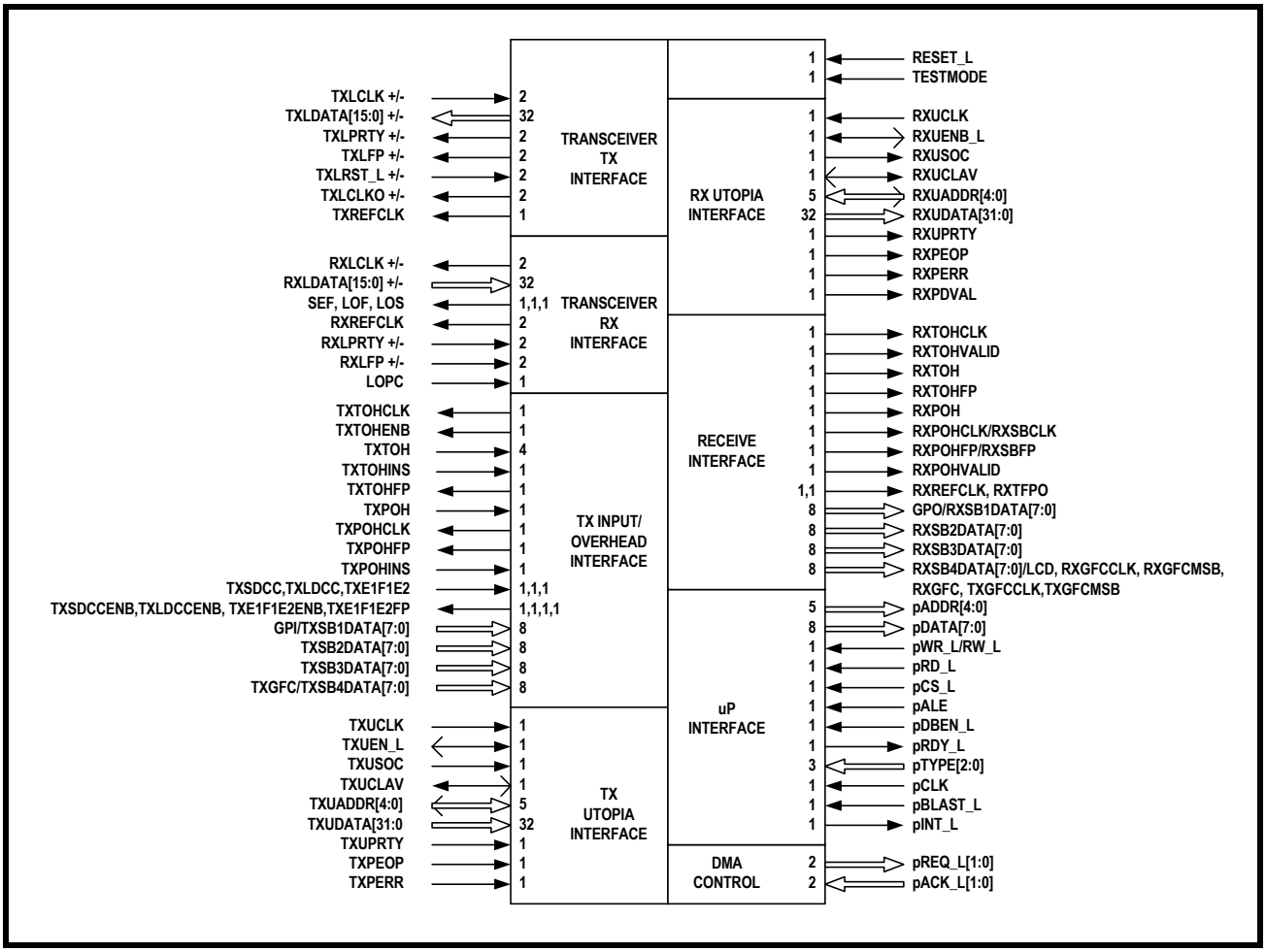
TOP VIEW

XRT95L51 (388 PINS)

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT95L51IB	388 Pin PBGA 35x35 mm, 26x26 Ball Matrix	-40°C to +85°C

FIGURE 4. SIGNAL DIAGRAM OF XRT95L51

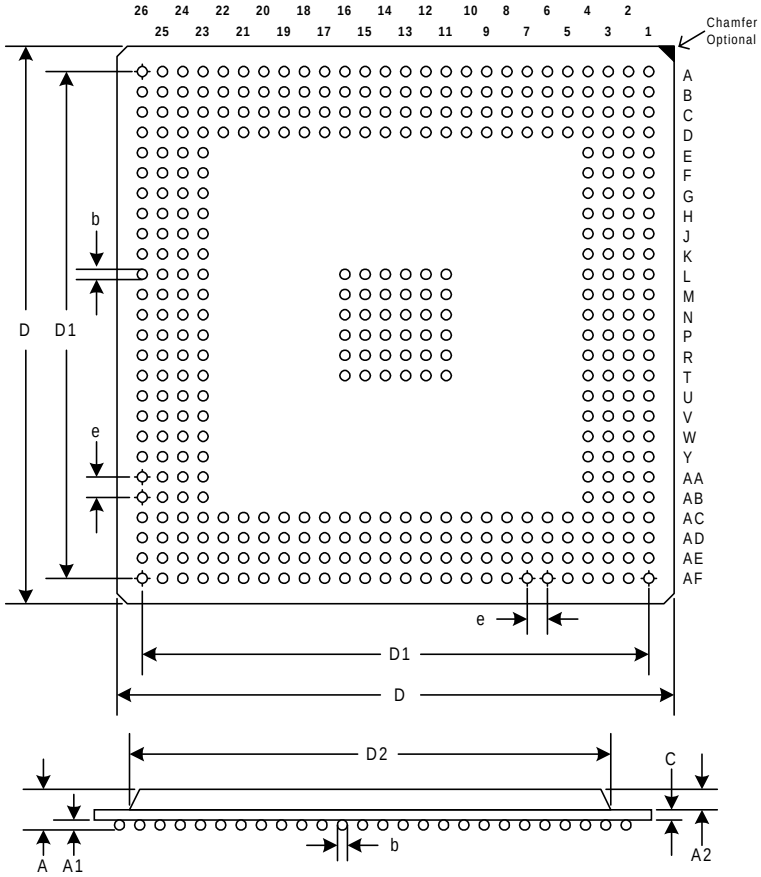


ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT95L51IB	388 Pin PBGA 35x35 mm, 26x26 Ball Matrix	-40°C to +85°C

PACKAGE DIMENSIONS

388 Ball Plastic Ball Grid Array
(35 x 35 mm PBGA)
Rev. 1.0



Symbol	Inches MIN	Inches MAX	Millimeters MIN	Millimeters MAX
A	0.075	0.106	1.90	2.70
A1	0.020	0.028	0.50	0.70
A2	0.039	0.051	1.00	1.30
b	0.024	0.035	0.60	0.90
C	0.016	0.028	0.40	0.70
D	1.370	1.386	34.80	35.20
D1	1.250BSC		31.75BSC	
D2	1.177	1.185	29.90	30.10
e	0.050BSC		1.27BSC	

Note: The control dimension is the millimeter column

REVISION HISTORY

NOTICE