

**10/9/8-bit 160MSPS D/A Converter**

**Descriptions**

A series of D/A converters CX20201A/CX20202A convert binary data into an analog signal at rates higher than 160 MHz. The devices include input data registers and have a capability of driving 75 ohms load. Three versions with linearity specifications of 10, 9 or 8 bits are available for each model.

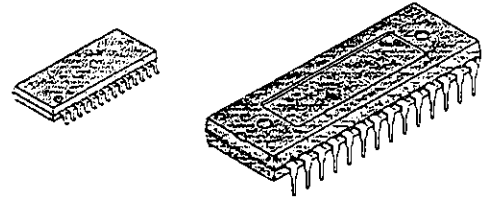
These D/A converter ICs can be used in signal processings which require high speed and high resolution D/A conversions such as high quality displays, high definition video systems, digital measurement instruments and radars.

CX20201A-1/CX20202A-1	10-bit
CX20201A-2/CX20202A-2	9-bit
CX20201A-3/CX20202A-3	8-bit

**Features**

- High speed 160 MHz
- High accuracy 10 bit (CX20201A-1/  
CX20202A-1)

28pin SOP(Plastic) 28pin DIP(Plastic)

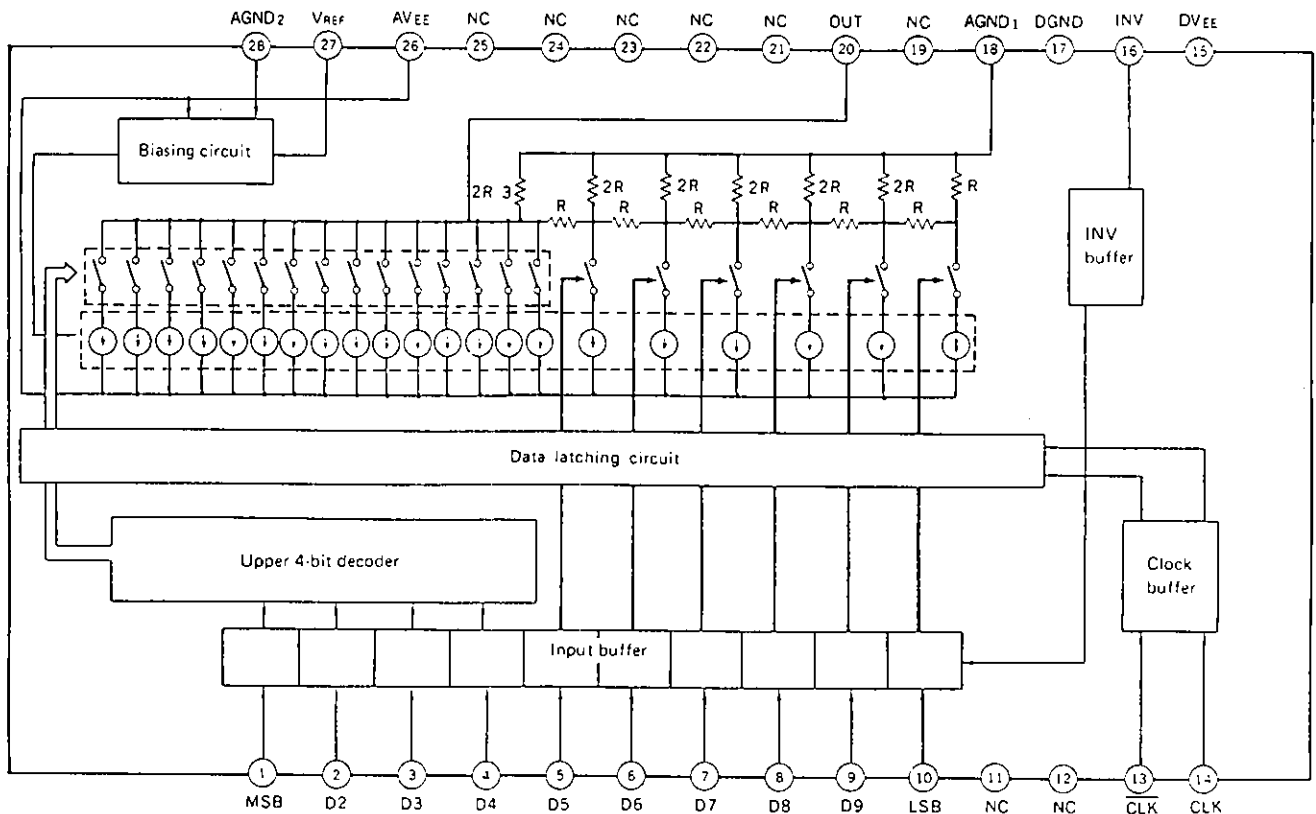


- Low glitch energy 15 pVsec
- Low power consumption 420 mW
- Logic invert input
- 75-Ω direct drive capability
- Analog multiplying function

**Structure**

Bipolar silicon monolithic IC.

**Block Diagram and Pin Configuration (Top View)**



**Absolute Maximum Ratings (Ta = 25°C)**

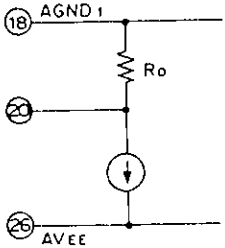
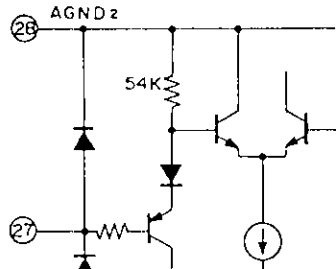
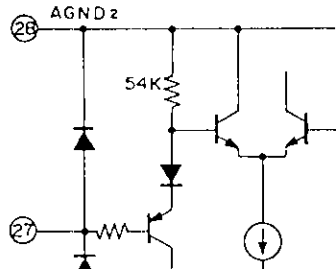
• Supply voltage	V <sub>EE</sub>	-7	V
• Digital input voltage	V <sub>I</sub>	+0.3 to V <sub>EE</sub>	V
• Reference input voltage	V <sub>REF</sub>	+0.3 to V <sub>EE</sub>	
• Analog output current	I <sub>OUT</sub>	20	mA
• Operating temperature	T <sub>ope</sub>	-20 to +75	°C
• Storage temperature	T <sub>stg</sub>	-55 to +150	°C
• Allowable power dissipation	P <sub>D</sub>		
	CX20201A-1/-2/-3	870	mW
	CX20202A-1/-2/-3	1430	mW

**Recommended Operating Conditions**

• Supply voltage	A <sub>VEE</sub> , D <sub>VEE</sub>	-4.75 to -5.45	V
	A <sub>VEE</sub> -D <sub>VEE</sub>	-0.05 to +0.05	V
• Digital input voltage	V <sub>IH</sub>	-1.0 to -0.7	V
	V <sub>IL</sub>	-1.9 to -1.6	V
• Reference input voltage	V <sub>REF</sub>	V <sub>EE</sub> +0.5 to	
		V <sub>EE</sub> +1.4	V
• Load resistance	R <sub>L</sub>	above 75	Ω
• Output voltage	V <sub>O(FS)</sub>	0.8 to 1.2	V

Pin Description

No.	Symbol	Equivalent circuit	Description
1 2 3 4 5 6 7 8 9 10	MSB D2 D3 D4 D5 D6 D7 D8 D9 LSB		Input pin for digital data. MSB and LSB are corresponded to the most significant bit and least significant bit, respectively. Pins not used should be left open or connected to DVEE.
11 12	NC		Non-connection
13 14	$\overline{\text{CLK}}$ CLK		Pins for clock inputs.
15	DVEE		Power supply pin for digital circuit.
16	INV		Code invert input pin which inverts the relationship between the binary code of digital data and D/A output voltage level.
17	DGND		Grounding pin for digital circuit.
18	AGND <sub>1</sub>		Grounding pin directly connected to the R-2R output resistor circuit network in the IC. Grounding for analog circuit system.
19	NC		Non-connection

No.	Symbol	Equivalent circuit	Description
20	OUT		D/A analog output.
21 22 23 24 25	NC		Non-connection
26	AVEE <sub>1</sub>		Power supply pin for analog circuit.
27	VREF		Bias pin which controls D/A output range. The output scale is set by the potential difference between VREF and AVEE.
28	AGND <sub>3</sub>		Grounding pin for analog circuit system other than the R-2R output resistor circuit network in the IC

Electrical Characteristics (1)  $T_a = 25^\circ\text{C}$ ,  $AV_{EE} = DV_{EE} = -5.2\text{V}$ ,  $AGND = DGND = 0\text{V}$ ,  $R_L = \infty$ ,  $V_{O(FS)} = -1\text{V}$

CX20201A-1/CX20202A-1

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		10		bit
Differential linearity error	ELD	-1/2		+1/2	LSB
Linearity error	ELI	-0.1		+0.1	% of FS
Settling time	$t_s$		5.2		ns

## CX20201A-2/CX20202A-2

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		9		bit
Differential linearity error	ELD	-1/2		+1/2	LSB
Linearity error	ELI	-0.1		+0.1	% of FS
Settling time	$t_s$		4.7		ns

## CX20201A-3/CX20202A-3

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		8		bit
Differential linearity error	ELD	-1/2		+1/2	LSB
Linearity error	ELI	-0.2		+0.2	% of FS
Settling time	$t_s$		4.3		ns

Electrical Characteristics (2)  $T_a = 25^\circ\text{C}$ ,  $A_{VEE} = D_{VEE} = -5.2\text{V}$ ,  $AGND = DGND = 0\text{V}$ ,  $R_L = \infty$ ,  
 $V_{O(FS)} = -1\text{V}$

Item	Symbol	Measuring condition*1	Min.	Typ.	Max.	Unit
Power supply current	CX20201A	$I_{EE}$	-60	-75	-90	mA
	CX20202A		-65	-82	-100	
Data input current (for upper 4 bits)	$I_{IH(U)}$	$V_{IH} = -0.89\text{V}$	0.1	1.5	6.0	$\mu\text{A}$
	$I_{IL(U)}$	$V_{IL} = -1.75\text{V}$	0.1	1.5	6.0	$\mu\text{A}$
Data input current (for lower 6 bits)	$I_{IH(L)}$	$V_{IH} = -0.89\text{V}$	0.1	0.75	3.0	$\mu\text{A}$
	$I_{IL(L)}$	$V_{IL} = -1.75\text{V}$	0	0.75	3.0	$\mu\text{A}$
Clock input current	$I_{CLKH}$	$V_{IH} = -0.89\text{V}$	2	23	70	$\mu\text{A}$
Invert input current	$I_{INVH}$	$V_{IH} = -0.89\text{V}$	0.1	1.5	6.0	$\mu\text{A}$
Reference input current	$I_{REF}$	$V_{REF} = -4.58\text{V}$	-3	-0.4	-0.1	$\mu\text{A}$
Output resistance	$R_O$	$I_O = -1\text{mA}$	52	65	78	$\Omega$
Maximum conversion rate	$f_c$	$R_L = 75\Omega$	160			MSPS
Output voltage full-scale deviation	$V_{O(FS)}$	$V_{REF} = -4.58\text{V}$	0.90	1.00	1.10	V
Set-up time	$t_{su}$		5.0			ns
Hold time	$t_{hd}$		1.0			ns

\*1 See Figs. 3 to 5.

Data for Typical Application

$T_a = 25^\circ\text{C}$ ,  $A_{VEE} = D_{VEE} = -5.2\text{V}$ ,  $AGND = DGND = 0\text{V}$ ,  $R_L = \infty$ ,  $V_{O(FS)} = -1\text{V}$

Item	Symbol	Measuring condition	Typ.	Unit
Output voltage zero offset	EZS	$R_L \cong 10\text{k}\Omega$	-7	mV
		$R_L = 75\Omega$	-7	
Output voltage full-scale temperature coefficient	$T_{C(FS)}$	$R_L \cong 10\text{k}\Omega$	-140	ppm/°C
		$R_L = 75\Omega$	-580	
Output voltage zero offset temperature coefficient	$T_{C(ZS)}$	$R_L \cong 10\text{k}\Omega$	16	$\mu\text{V}/^\circ\text{C}$
Glitch energy	GE	Digital ramp	15	pVsec
Rise time	$t_r$	$R_L = 75\Omega$	1.5	ns
Fall time	$t_f$		1.5	ns
Propagation delay	$t_d$		3.8	ns
Band width for multiplying	$BW_{MUL}$	$R_L = 75\Omega$ , -3dB	14	MHz

Timing Chart

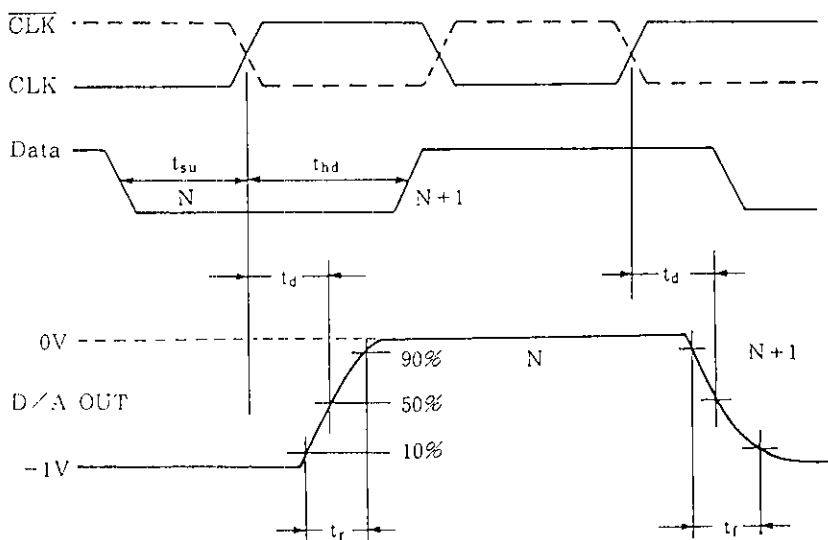


Fig. 1

Input Coding Table

Input code	Output code (V)	
	INV = 1	INV = 0
0 0 0 ..... 0 0	0	-1
⋮	⋮	⋮
0 1 1 ..... 1 1	-0.5	-0.5
1 0 0 ..... 0 0	⋮	⋮
⋮	⋮	⋮
1 1 1 ..... 1 1	-1	0

Measuring Conditions for Current Consumption, Input Current and Output Resistance  
(See Fig. 2.)

Test item	Symbol	Switch condition																				Test point		
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20		S21	
Current consumption	$I_{EE}$	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	b	b	b	b	b		I1	
Data input current for upper 4 bits (H level)	$I_{IH(U)}$	a	b	b	b																		I2	
		b	a	b	b	b	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	b		
		b	b	a	b																			
		b	b	b	a																			
Data input current for lower 4 bits (L level)	$I_{IL(U)}$	a	b	b	b																		I2	
		b	a	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b		
		b	b	a	b																			
		b	b	b	a																			
Data input current for upper 6 bits (H level)	$I_{IH(L)}$					a	b	b	b	b	b												I2	
						b	a	b	b	b	b													
		b	b	b	b	b	b	a	b	b	b	a	b	b	b	b	b	b	b	b	b	b		
						b	b	b	b	a	b	b												
						b	b	b	b	b	a	b												
						b	b	b	b	b	a													
Data input current for lower 6 bits (L level)	$I_{IL(L)}$					a	b	b	b	b	b												I2	
						b	a	b	b	b	b													
		b	b	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	b	b	b	b		
						b	b	b	b	a	b	b												
						b	b	b	b	b	a	b												
Clock input current (H level)	$I_{CLKH}$	b	b	b	b	b	b	b	b	b	b	a	b	b	a	b	b	b	b	b	b	I3		
Clock-bar input current (H level)	$I_{\overline{CLKH}}$	b	b	b	b	b	b	b	b	b	b	b	a	a	b	b	b	b	b	b	b	I4		
Invert input current (H level)	$I_{INVH}$	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	b	b	b	I5		
Reference input current	$I_{REF}$	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	I6		
Output resistance	$R_O$	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	V1		

Electrical Characteristics Test Circuit

Test Circuit for Current Consumption, Input Current and Output Resistance

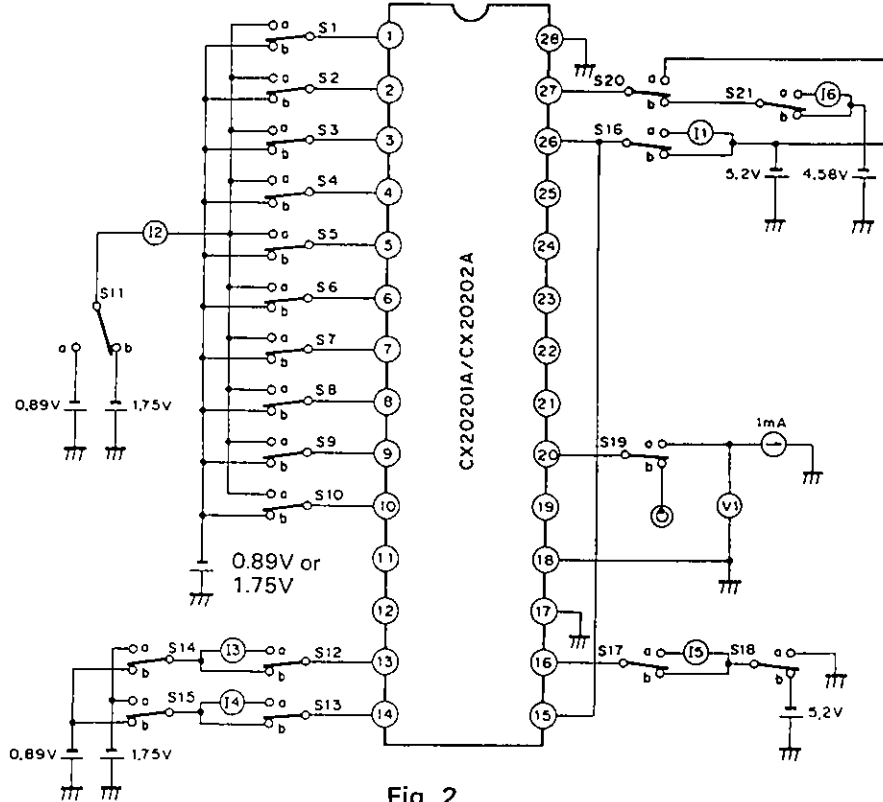
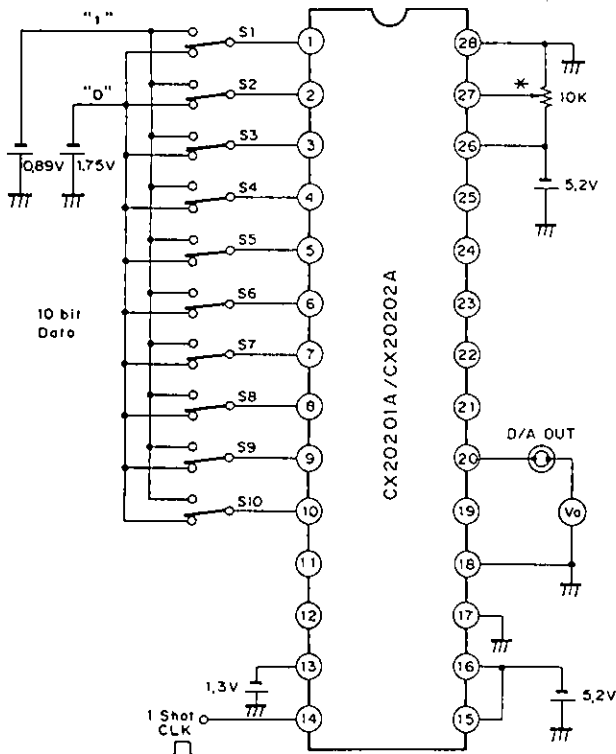


Fig. 2

Test Circuit for Differential Linearity Error and Linearity Error



Linearity errors are measured as follows.

S1	S2	S3	.....	S9	S10	D/A out
0	0	0	.....	0	0	$V_0$
0	0	0	.....	0	1	$V_1$
0	0	0	.....	1	0	$V_2$
			⋮			⋮
1	1	1	.....	1	1	$V_{1023}$

Linearity error      Differential linearity error

$V_0$	
$V_1$	$V_1 - V_0$
$V_2$	$V_2 - V_1$
$V_4$	$V_4 - V_3$
$V_6$	$V_6 - V_5$
$V_{16}$	$V_{16} - V_{15}$
$V_{32}$	$V_{32} - V_{31}$
$V_{64}$	$V_{64} - V_{63}$
$V_{128}$	$V_{128} - V_{127}$
$V_{192}$	$V_{192} - V_{191}$
⋮	⋮
$V_{960}$	$V_{960} - V_{959}$
$V_{1023}$	

\* Adjust so that the full scale of DC voltage at Pin 20 becomes 1.023V, that is, to satisfy  $V_0 - V_{1023} = 1.023V$ .

Fig. 3

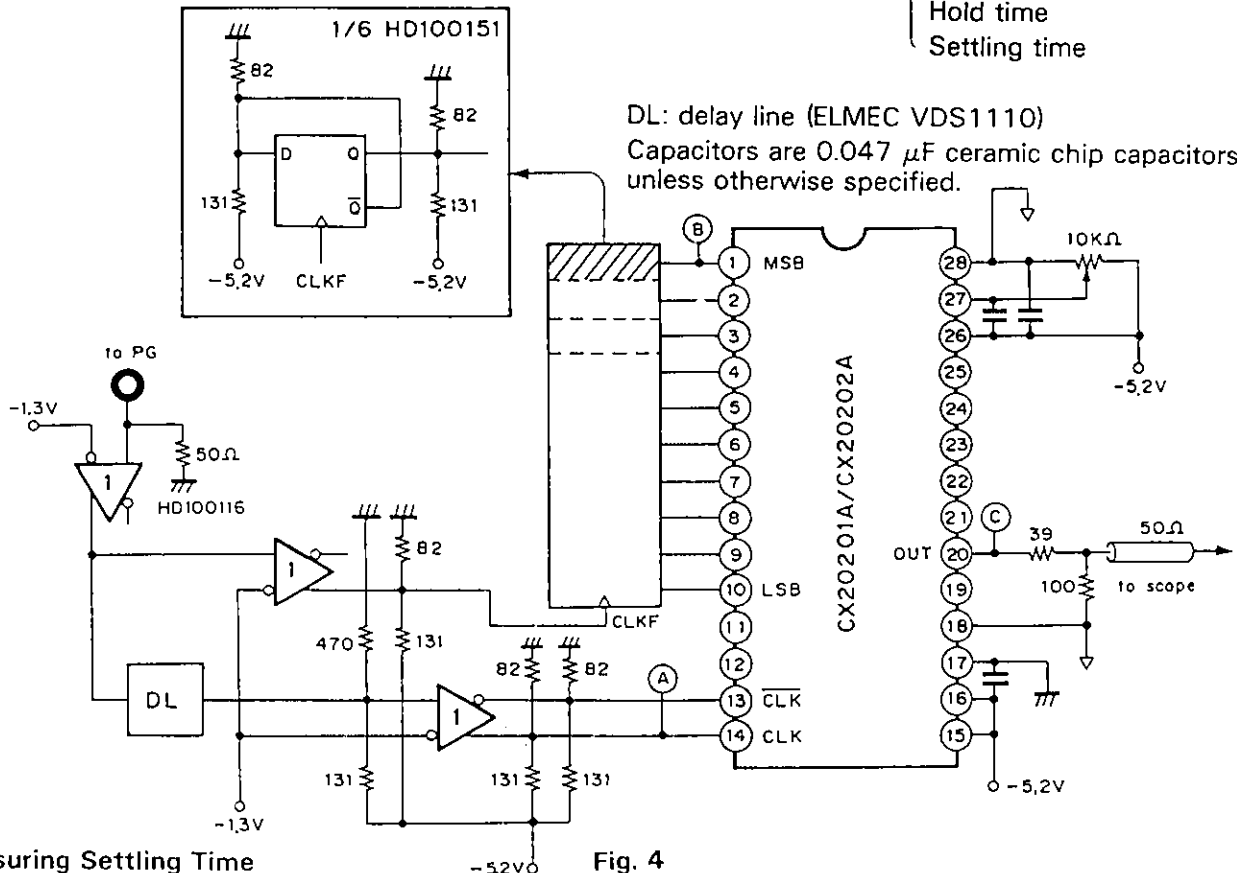
Errors at individual measurement points are calculated according to the following definition.

$$(V_{1023} - V_0)/1023 = V_0(FS)/1023 \equiv 1 \text{ LSB.}$$



Test circuits for

- Maximum conversion rate
- Rise time
- Fall time
- Propagation delay
- Set-up time
- Hold time
- Settling time



**Measuring Settling Time**

Settling time is measured as follows. The relationship between  $V$  and  $V_0(FS)$  as shown in the D/A output waveform in Fig. 5 is expressed as

$$V = V_0(FS) (1 - e^{-t/\tau})$$

The settling time for respective accuracy of 10 , 9 and 8-bit is specified as

$$V = 0.9995 V_0(FS)$$

$$V = 0.999 V_0(FS)$$

$$V = 0.998 V_0(FS)$$

which results in the following:

$$t_s = 7.60\tau \quad \text{for 10-bit,}$$

$$t_s = 6.93\tau \quad \text{for 9-bit, and}$$

$$t_s = 6.24\tau \quad \text{for 8-bit}$$

Rise time ( $t_r$ ) and fall time ( $t_f$ ) are defined as the time interval to slew from 10% to 90% of full scale voltage ( $V_0(FS)$ ):

$$V = 0.1 V_0(FS)$$

$$V = 0.9 V_0(FS)$$

and calculated as  $t_r = t_f = 2.20 \tau$ .

The settling time is obtained by combining these expressions:

$$t_s = 3.45t_r \quad \text{for 10-bit,}$$

$$t_s = 3.15t_r \quad \text{for 9-bit, and}$$

$$t_s = 2.84t_r \quad \text{for 8-bit}$$

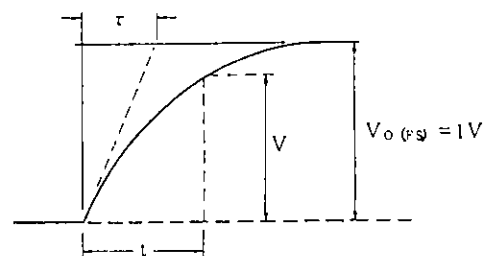


Fig. 5

Test Circuit for Multiplying Band Width

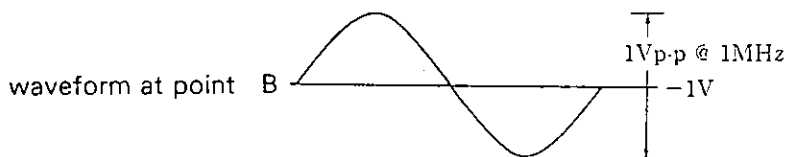
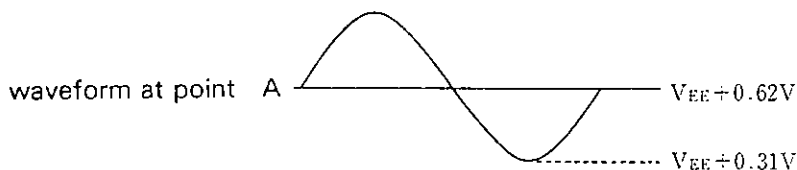
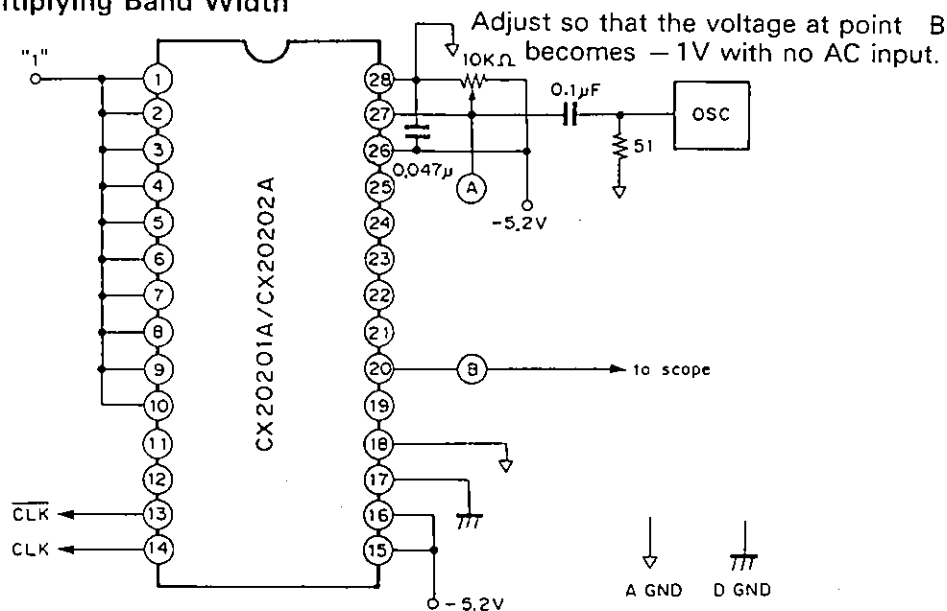
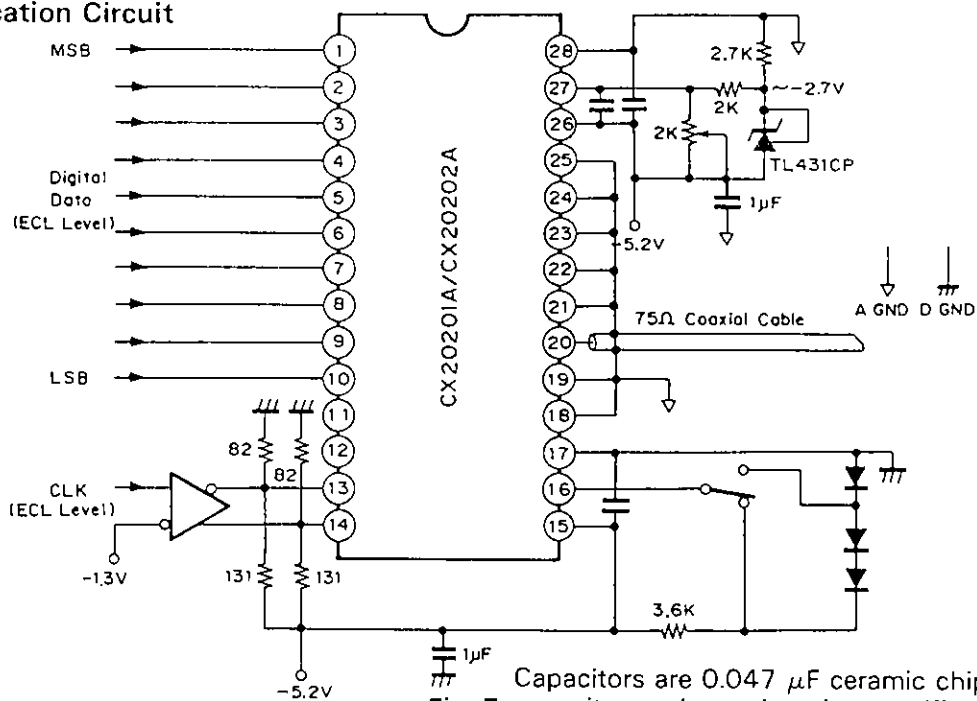


Fig. 6

Typical Application Circuit



Capacitors are 0.047 μF ceramic chip Fig. 7 capacitors unless otherwise specified.

## Notes on Applications

### (1) Setting of full-scale output voltage

The full-scale output voltage ( $V_{O(FS)}$ ) is set by the pin 27 ( $V_{REF}$ ).  $V_{O(FS)}$  varies in proportion to the voltage difference between pin 27 and pin 26 ( $A_{VEE}$ ) as shown in Fig. 9.

$V_{O(FS)}$  can be set by simply dividing the supply voltage using resistors as shown in Fig. 8, but in this simple set up the voltage deviation of the supply voltage result in a deviation of  $V_{O(FS)}$ . This influence can be avoided by using a stabilization circuit as shown in Fig. 7 to allow stable full-scale output.

Pin 27 ( $V_{REF}$ ) should be stabilized against high-frequency noise by sufficient by passing using a capacitor with low lead inductance such as ceramic chip capacitors. The stabilization capacitor should be inserted between pin 27 ( $V_{REF}$ ) and pin 26 ( $A_{VEE}$ ) as  $V_{O(FS)}$  is direct proportion to the voltage across these two terminals.

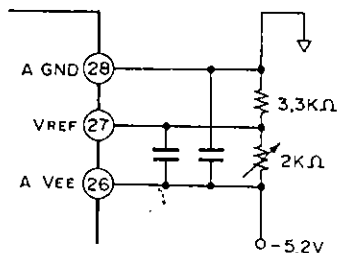


Fig. 8

### (2) Noise reduction

An external digital noise should be minimized because the system handles small analog voltage (1 LSB corresponds 1 mV of analog output voltage for 10 bit resolution). Refer to the following notes to minimize the system noise contamination.

- Ground plane and VEE plane on a printed circuit board should be made as wide as possible to reduce parasitic inductance and resistance.
- The patterns AGND and DGND should be separated on the printed circuit board.  $A_{VEE}$  and  $D_{VEE}$  should be separated too. The connections between analog system and digital system are to be made at the I/O ports of the printed circuit board.
- $A_{VEE}$  and  $D_{VEE}$  should be bypassed to respective GND by using a tantalum capacitor of 1  $\mu$ F and a ceramic chip capacitor of 47  $\mu$ F positioned as close as to terminals of the IC.
- Pins not in sure are to be connected to the ground plane.

### (3) Load resistance and temperature coefficient

Temperature coefficient of the full-scale output voltage and zero offset voltage depend on the load resistance (value and type). Generally, the larger the load resistance the better the temperature coefficient value. Temperature characteristics at  $R_L \geq 10 \text{ k}\Omega$  and  $R_L = 75 \Omega$  are shown in Fig. 10.

### (4) Input data and internal latching circuit

CX20201A/CX20202A incorporates a latching circuit as shown in the block diagram. This latching circuit has a two-stage configuration (master-slave type) and fetches input data only at the rising edge of the clock; the output is not affected by the changes in input data at any other timings. This mechanism allows stable operation against any changes in input data at any timings, except for the set-up time immediately before and the hold time immediately after the clock change from L to H.

### (5) Driving input data and clock

CX20201A/CX20202A are designed to be operated at very high speed. It is, therefore, necessary to drive it with a high-speed ICs such as an ECL100K for full performance. Also the output port of the data and clock drivers should be terminated with 50- $\Omega$  systems. See Figs. 4 and 7.

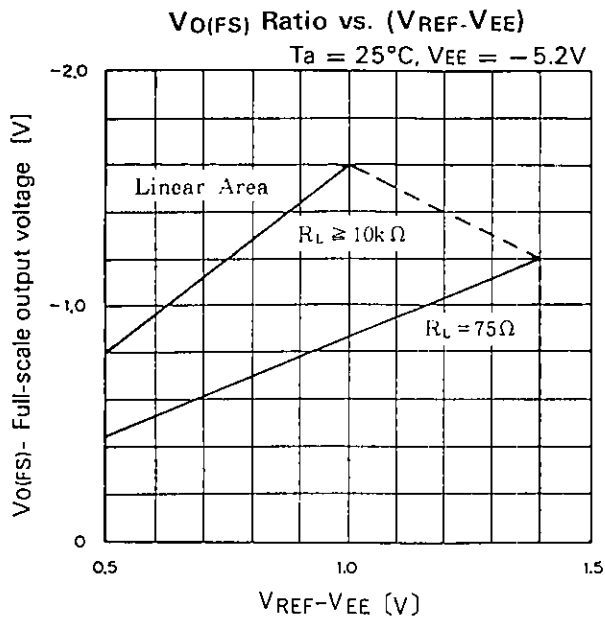


Fig. 9

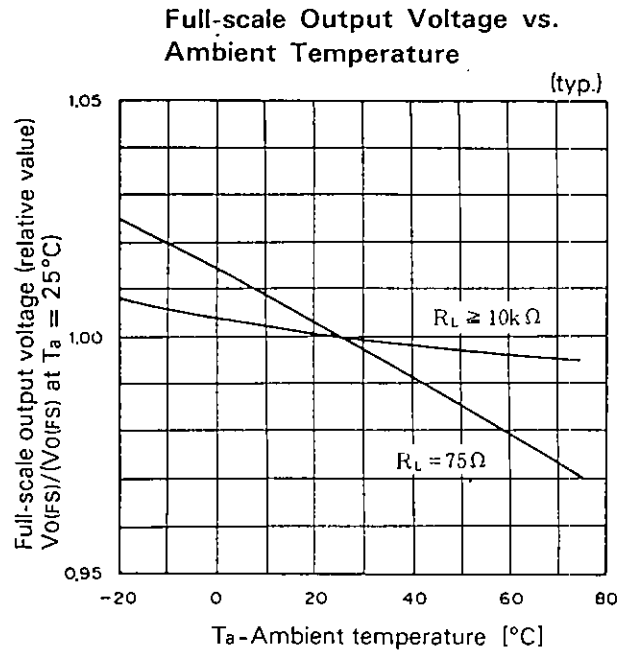


Fig. 10

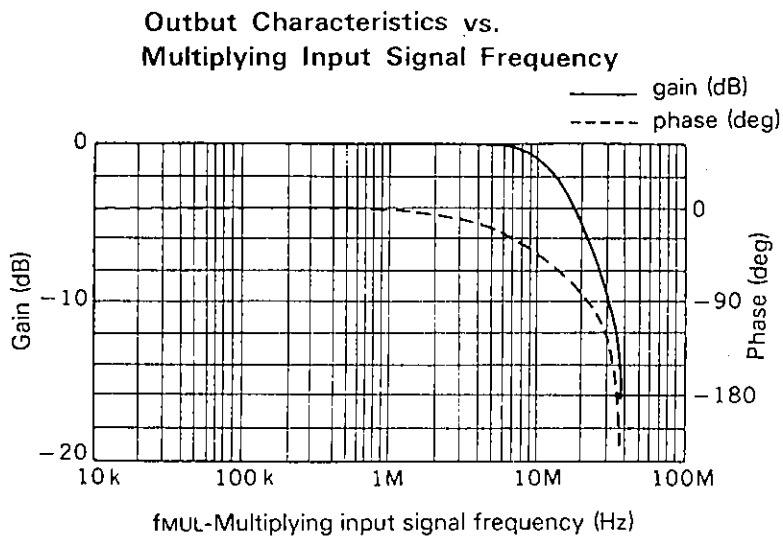


Fig. 11

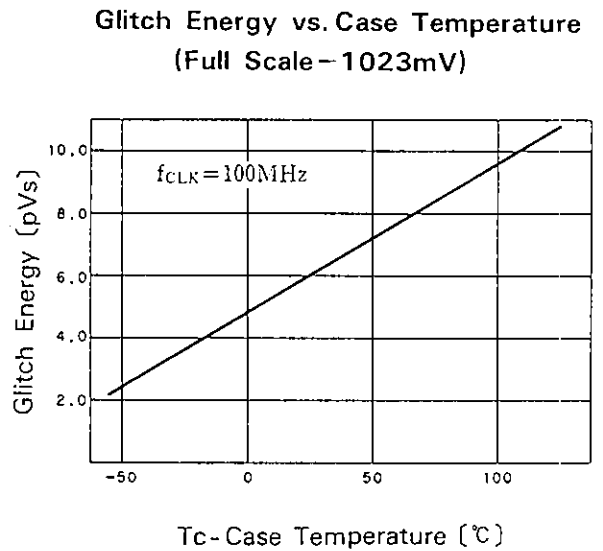
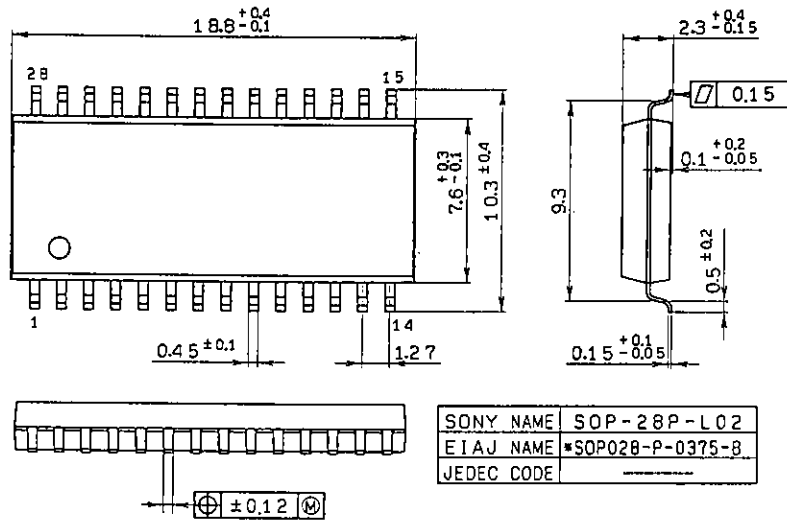


Fig. 12

Package Outline Unit : mm

CX20201A 28pin SOP(Plastic) 375mil 0.6g



CX20202A 28pin DIP(Plastic) 600mil 4.2g

