



## Timing-Safe™ Peak EMI Reduction IC

### General Features

- Clock distribution with Timing-Safe™ Peak EMI Reduction
- Input frequency range: 20MHz - 50MHz
- Multiple low skew Timing-safe™ Outputs:  
PCS3P623Z05: 5 Outputs  
PCS3P623Z09: 9 Outputs
- External Input-Output Delay Control option
- Supply Voltage: 3.3V±0.3V
- Commercial and Industrial temperature range
- Packaging Information:  
ASM3P623Z05: 8 pin SOIC, and TSSOP  
ASM3P623Z09: 16 pin SOIC, and TSSOP
- True Drop-in Solution for Zero Delay Buffer, ASM5P2305A / 09A

### Functional Description

PCS3P623Z05/09 is a versatile, 3.3V Zero-delay buffer designed to distribute Timing-Safe™ clocks with Peak EMI reduction. PCS3P623Z05 is an eight-pin version, accepts one reference input and drives out five low-skew Timing-Safe™ clocks. PCS3P623Z09 accepts one reference input and drives out nine low-skew Timing-Safe™ clocks.

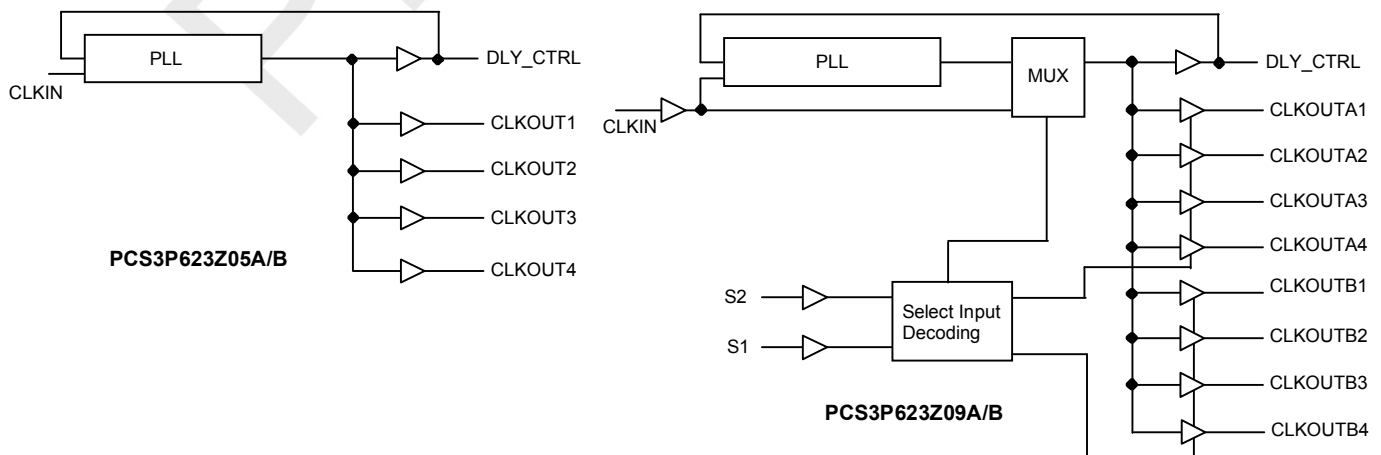
PCS3P623Z05/09 has a DLY\_CTRL for adjusting the Input-Output clock delay, depending upon the value of capacitor connected at this pin to GND.

PCS3P623Z05/09 operates from a 3.3V supply and is available in two different packages, as shown in the ordering information table, over commercial and Industrial temperature range.

### Application

PCS3P623Z05/09 is targeted for use in Displays and memory interface systems.

### General Block Diagram



## Spread Spectrum Frequency Generation

The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi-layer PCBs, etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The PCS3P623Z05/09 uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation.

## Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the DLY\_CTRL pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

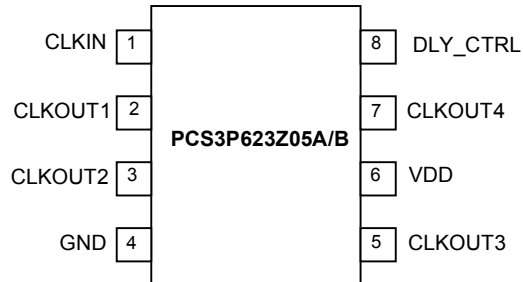
For applications requiring zero input-output delay, all outputs, including DLY\_CTRL, must be equally loaded. Even if DLY\_CTRL is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero input-output delay.

## Timing-Safe™ technology

Timing-Safe™ technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

# PCS3P623Z05A/B and PCS3P623Z09A/B

## Pin Configuration for PCS3P623Z05A/B



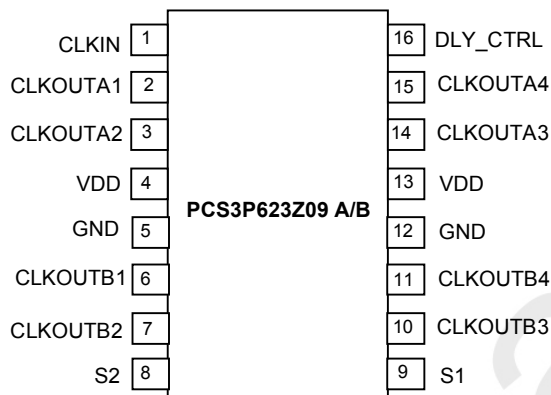
## Pin Description for PCS3P623Z05A/B

Pin #	Pin Name	Type	Description
1	CLKIN <sup>1</sup>	I	External reference Clock input, 5V tolerant input
2	CLKOUT1 <sup>2</sup>	O	Buffered clock output <sup>4</sup>
3	CLKOUT2 <sup>2</sup>	O	Buffered clock output <sup>4</sup>
4	GND	P	Ground
5	CLKOUT3 <sup>2</sup>	O	Buffered clock output <sup>4</sup>
6	VDD	P	3.3V supply
7	CLKOUT4 <sup>2</sup>	O	Buffered clock output <sup>4</sup>
8	DLY_CTRL	O	External Input-Output Delay control. This pin can be used as clock output <sup>4</sup>

- Notes:
1. Weak pull down
  2. Weak pull-down on all outputs
  3. Weak pull-up on these Inputs
  4. Buffered clock output is Timing-Safe™

# PCS3P623Z05A/B and PCS3P623Z09A/B

## Pin Configuration for PCS3P623Z09A/B



## Pin Description for PCS3P623Z09A/B

Pin #	Pin Name	Pin Type	Description
1	CLKIN <sup>1</sup>	I	External reference Clock input, 5V tolerant input
2	CLKOUTA1 <sup>2</sup>	O	Buffered clock Bank A output <sup>4</sup>
3	CLKOUTA2 <sup>2</sup>	O	Buffered clock Bank A output <sup>4</sup>
4	VDD	P	3.3V supply
5	GND	P	Ground
6	CLKOUTB1 <sup>2</sup>	O	Buffered clock Bank B output <sup>4</sup>
7	CLKOUTB2 <sup>2</sup>	O	Buffered clock Bank B output <sup>4</sup>
8	S2 <sup>3</sup>	I	Select input, bit 2. See <i>Select Input Decoding table for PCS3P623Z09</i> for more details
9	S1 <sup>3</sup>	I	Select input, bit 1. See <i>Select Input Decoding table for PCS3P623Z09</i> for more details
10	CLKOUTB3 <sup>2</sup>	O	Buffered clock Bank B output <sup>4</sup>
11	CLKOUTB4 <sup>2</sup>	O	Buffered clock Bank B output <sup>4</sup>
12	GND	P	Ground
13	VDD	P	3.3V supply
14	CLKOUTA3 <sup>2</sup>	O	Buffered clock Bank A output <sup>4</sup>
15	CLKOUTA4 <sup>2</sup>	O	Buffered clock Bank A output <sup>4</sup>
16	DLY_CTRL <sup>2</sup>	O	External Input-Output Delay control. This pin can be used as clock output

Notes: 1. Weak pull down

2. Weak pull-down on all outputs

3. Weak pull-up on these Inputs

4. Buffered clock output is Timing-Safe™

# PCS3P623Z05A/B and PCS3P623Z09A/B

## Select Input Decoding table for PCS3P623Z09

S2	S1	CLKOUT A1 - A4	CLKOUT B1 - B4	DLY_CTRL <sup>1</sup>	Output Source	PLL Shut-Down
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Notes: This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and the Output

## Spread Spectrum Control and Input-Output Skew Table

Frequency (MHz)	Device	Deviation (±%)	Input-Output Skew (±T <sub>SKREW</sub> )
32	PCS3P623Z05A / 09A	0.125	0.125
	PCS3P623Z05B / 09B	0.25	0.25

Note: T<sub>SKREW</sub> is measured in units of the Clock Period

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage to Ground Potential	-0.5 to +4.6	V
VIN	DC Input Voltage (CLKIN)	-0.5 to +7	
T <sub>STG</sub>	Storage temperature	-65 to +125	°C
T <sub>s</sub>	Max. Soldering Temperature (10 sec)	260	°C
T <sub>J</sub>	Junction Temperature	150	°C
T <sub>DV</sub>	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

## Operating Conditions

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)	-40	+85	°C
C <sub>L</sub>	Load Capacitance		30	pF
C <sub>IN</sub>	Input Capacitance		7	pF

# PCS3P623Z05A/B and PCS3P623Z09A/B

## Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Input LOW Voltage <sup>5</sup>				0.8	V
V <sub>IH</sub>	Input HIGH Voltage <sup>5</sup>		2.0			V
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0V			50	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = VDD			100	μA
V <sub>OL</sub>	Output LOW Voltage <sup>6</sup>	I <sub>OL</sub> = 8mA			0.4	V
V <sub>OH</sub>	Output HIGH Voltage <sup>6</sup>	I <sub>OH</sub> = -8mA	2.4			V
I <sub>DD</sub>	Supply Current	Unloaded outputs			27	mA
Z <sub>o</sub>	Output Impedance			23		Ω

Notes: 5. CLKIN input has a threshold voltage of VDD/2

6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Switching Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Frequency		20		50	MHz
Output Frequency	30pF load	20		50	MHz
Duty Cycle <sup>7,8</sup> = (t <sub>2</sub> / t <sub>1</sub> ) * 100	Measured at VDD/2	40	50	60	%
Output Rise Time <sup>7,8</sup>	Measured between 0.8V and 2.0V			2.5	nS
Output Fall Time <sup>7,8</sup>	Measured between 2.0V and 0.8V			2.5	nS
Output-to-output skew <sup>7,8</sup>	All outputs equally loaded			250	pS
Delay, CLKIN Rising Edge to CLKOUT Rising Edge <sup>8</sup>	Measured at VDD /2			±350	pS
Device-to-Device Skew <sup>8</sup>	Measured at VDD/2 on the CLKOUT pins of the device			700	pS
Cycle-to-Cycle Jitter <sup>7,8</sup>	Loaded outputs			±250	pS
PLL Lock Time <sup>8</sup>	Stable power supply, valid clock presented on CLKIN pin			1.0	mS

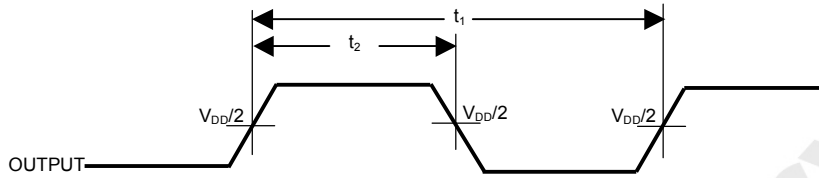
Notes: 7. All parameters specified with 30pF loaded outputs.

8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

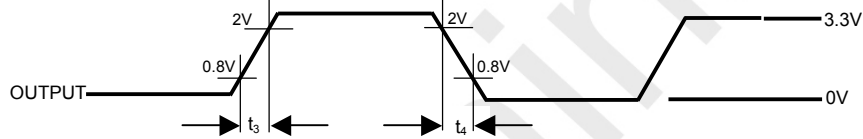
# PCS3P623Z05A/B and PCS3P623Z09A/B

## Switching Waveforms

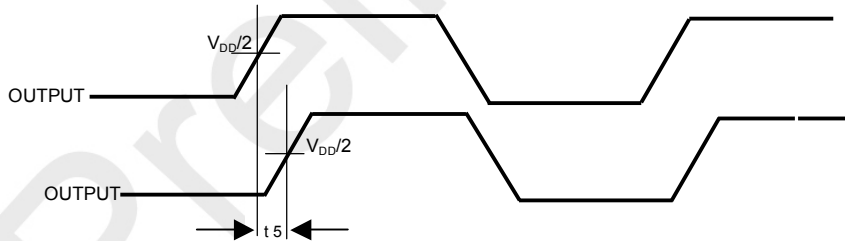
### Duty Cycle Timing



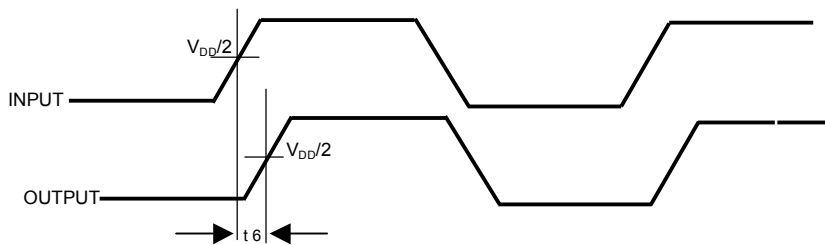
### All Outputs Rise/Fall Time



### Output - Output Skew

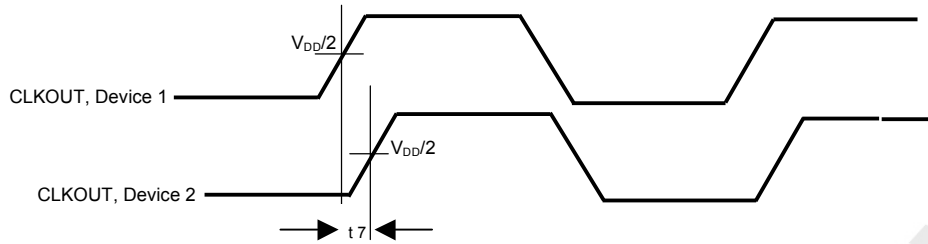


### Input - Output Propagation Delay

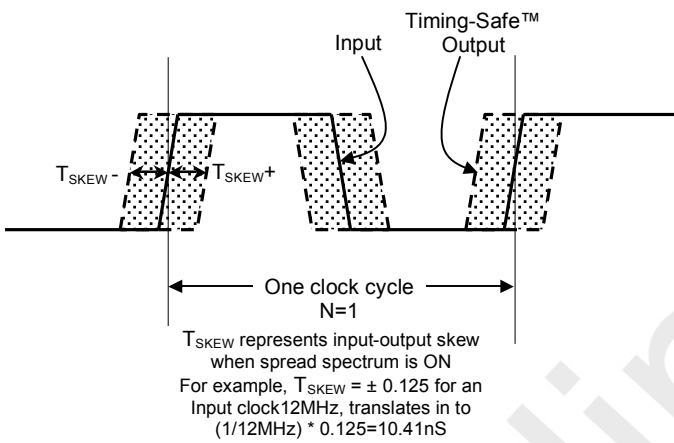


# PCS3P623Z05A/B and PCS3P623Z09A/B

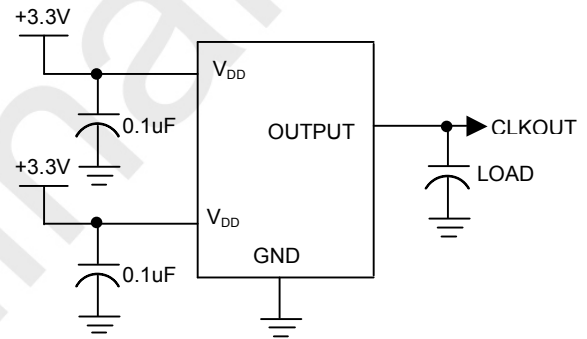
## Device - Device Skew



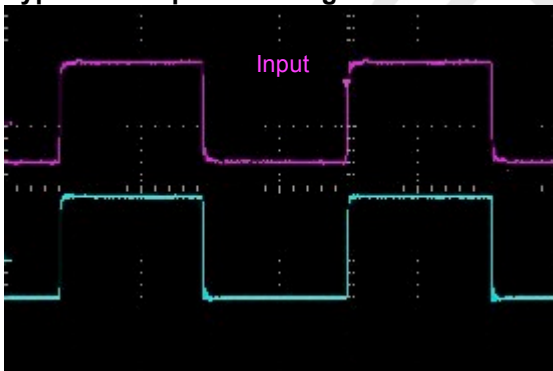
## Input - Output Skew



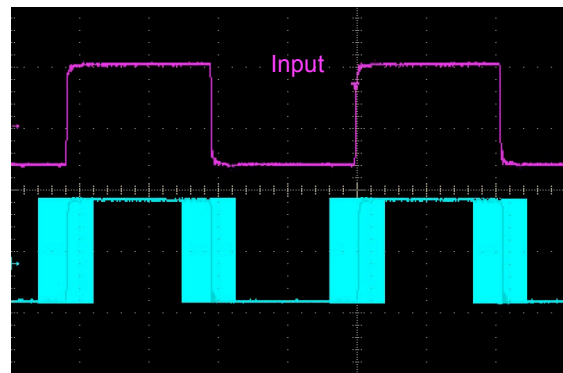
## Test Circuit



## Typical example of Timing-Safe™ waveform



CLKOUT with SSOFF



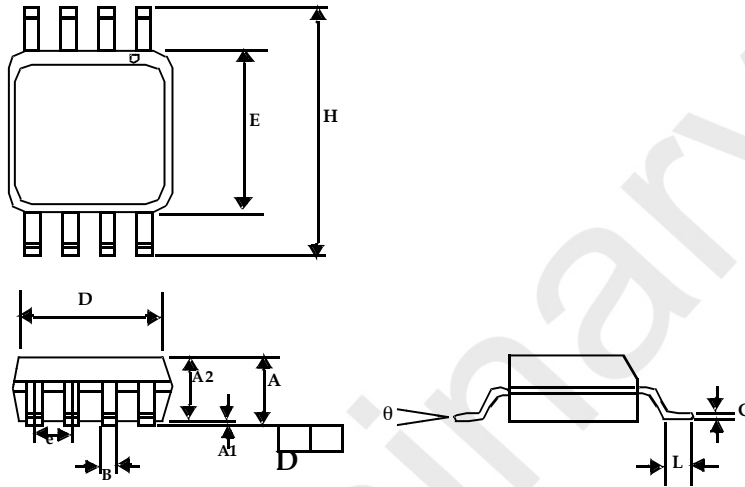
Timing-Safe™ CLKOUT



# PCS3P623Z05A/B and PCS3P623Z09A/B

## Package Information

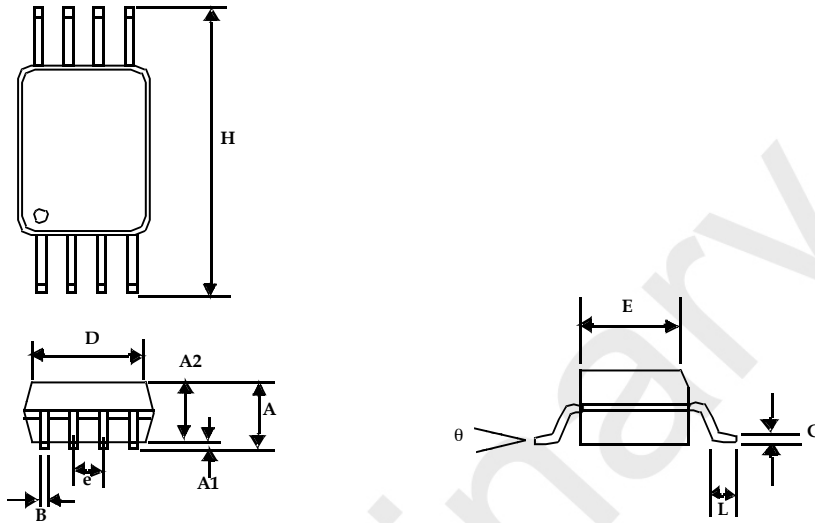
### 8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

# PCS3P623Z05A/B and PCS3P623Z09A/B

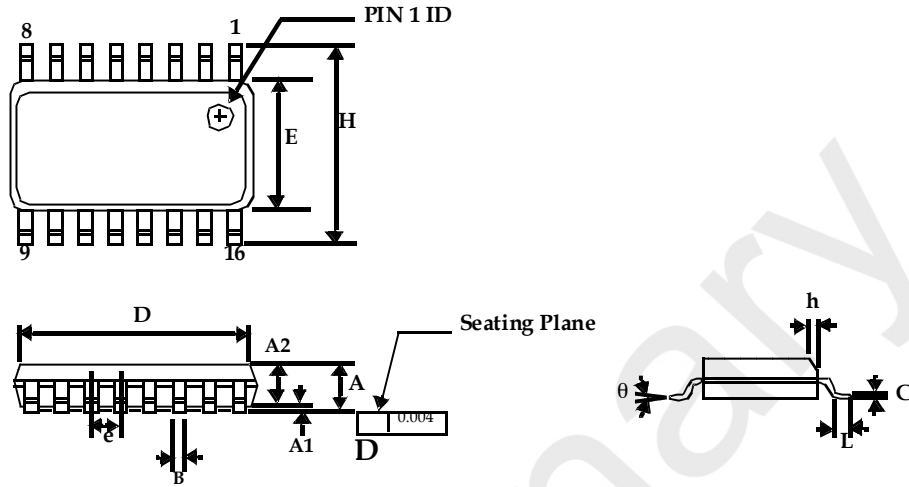
## 8-lead TSSOP (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
$\theta$	0°	8°	0°	8°

# PCS3P623Z05A/B and PCS3P623Z09A/B

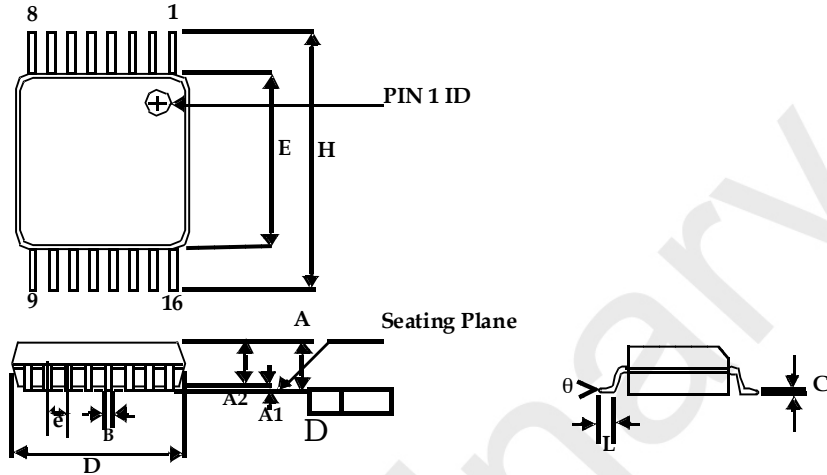
## 16-lead (150 Mil) Molded SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	0.059	1.25	1.50
B	0.013	0.022	0.33	0.53
C	0.008	0.012	0.19	0.27
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.40	0.89
$\theta$	0°	8°	0°	8°

# PCS3P623Z05A/B and PCS3P623Z09A/B

## 16-lead TSSOP (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.030	0.50	0.75
$\theta$	0°	8°	0°	8°

## PCS3P623Z05A/B and PCS3P623Z09A/B

### Ordering Code

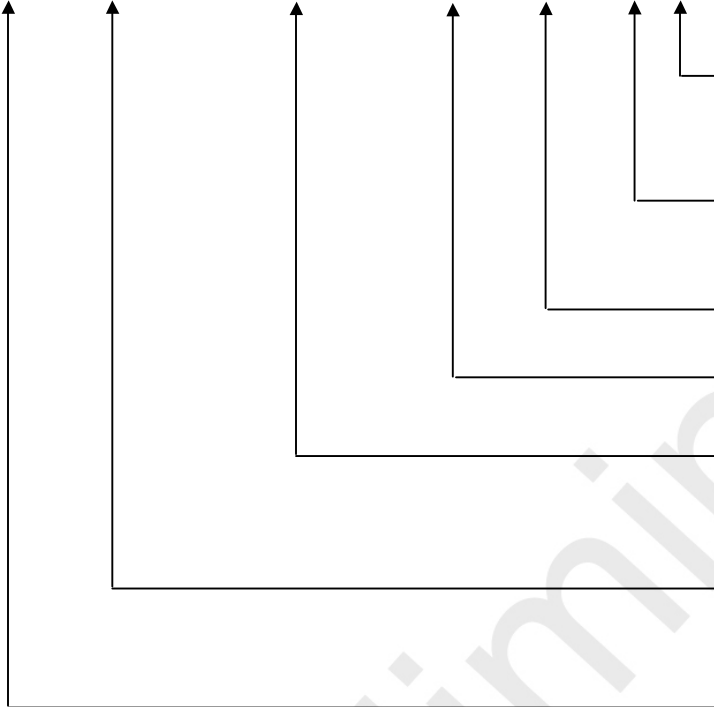
Ordering Code	Marking	Package Type	Temperature
PCS3P623Z0xyG-08-ST	3P623Z0xyG	8-pin 150-mil SOIC-TUBE, Green	Commercial
PCS3I623Z0xyG-08-ST	3I623Z0xyG	8-pin 150-mil SOIC-TUBE, Green	Industrial
PCS3P623Z0xyG-08-SR	3P623Z0xyG	8-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
PCS3I623Z0xyG-08-SR	3I623Z0xyG	8-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
PCS3P623Z0xyG-08-TT	3P623Z0xyG	8-pin 4.4-mm TSSOP - TUBE, Green	Commercial
PCS3I623Z0xyG-08-TT	3I623Z0xyG	8-pin 4.4-mm TSSOP - TUBE, Green	Industrial
PCS3P623Z0xyG-08-TR	3P623Z0xyG	8-pin 4.4-mm TSSOP - TAPE & REEL, Green	Commercial
PCS3I623Z0xyG-08-TR	3I623Z0xyG	8-pin 4.4-mm TSSOP - TAPE & REEL, Green	Industrial
PCS3P623Z0xyG-16-ST	3P623Z0xyG	16-pin 150-mil SOIC-TUBE, Green	Commercial
PCS3I623Z0xyG-16-ST	3I623Z0xyG	16-pin 150-mil SOIC-TUBE, Green	Industrial
PCS3P623Z0xyG-16-SR	3P623Z0xyG	16-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
PCS3I623Z0xyG-16-SR	3I623Z0xyG	16-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
PCS3P623Z0xyG-16-TT	3P623Z0xyG	16-pin 4.4-mm TSSOP - TUBE, Green	Commercial
PCS3I623Z0xyG-16-TT	3I623Z0xyG	16-pin 4.4-mm TSSOP - TUBE, Green	Industrial
PCS3P623Z0xyG-16-TR	3P623Z0xyG	16-pin 4.4-mm TSSOP - TAPE & REEL, Green	Commercial
PCS3I623Z0xyG-16-TR	3I623Z0xyG	16-pin 4.4-mm TSSOP - TAPE & REEL, Green	Industrial

Note: x=5 / 9; y=A / B

# PCS3P623Z05A/B and PCS3P623Z09A/B

## Device Ordering Information

PCS3P623Z0xyG-08-TR




R = Tape & Reel, T = Tube or Tray		
O = TSOT23 S = SOIC T = TSSOP A = SSOP V = TVSOP B = BGA Q = QFN	U = MSOP E = TQFP L = LQFP U = MSOP P = PDIP D = QSOP X = SC-70	J=TSOT26 C=TDFN (2X2) COL
DEVICE PIN COUNT		
F = LEAD FREE AND RoHS COMPLIANT PART G = GREEN PACKAGE, LEAD FREE, and RoHS		
PART NUMBER		
X= Automotive (-40C to +125C)	I= Industrial (-40C to +85C)	P or n/c = Commercial (0C to +70C)
1 = Clock Generator 2 = Non PLL based 3 = EMI Reduction 4 = DDR support products 5 = STD Zero Delay Buffer	6 = Power Management 7 = Power Management 8 = Power Management 9 = Hi Performance 0 = Reserved	
ON Semiconductor Mixed Signal Product		

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

# PCS3P623Z05A/B and PCS3P623Z09A/B

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. U.S. Patent Pending; Timing-Safe and Active Bead are trademarks of PulseCore Semiconductor, a wholly owned subsidiary of ON Semiconductor. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855  
Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative