REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to 1.2.1. Made technical changes to table I. Added a square chip carrier package to 1.2.2. Changes to figure 1 and figure 4. Added vendor CAGE number 59621 for the square chip carrier package.	91-10-18	Monica L. Poelking
B	Added device types 05 through 08. Made technical changes to table I. Added CAGE number 65896 for device types 05 through 08. Editorial changes throughout.	92-06-19	Tim Noh
C	Changes made in accordance with NOR 5962-R310-92	92-09-11	Monica L. Poelking
D	Changes made in accordance with NOR 5962-R113-93	93-03-29	Monica L. Poelking
E	Changes made in accordance with NOR 5962-R199-96	96-09-25	Monica L. Poelking
F	Updated boilerplate and made editorial changes throughout. - LTG	00-05-30	Monica L. Poelking
G	Updated boilerplate to MIL-PRF-38535 requirements. - CFS	05-08-15	Thomas M. Hess

REV																				
SHEET																				
REV	G																			
SHEET	15																			

REV STATUS	REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Phu Nguyen

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Tim H. Noh

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
88-11-07

REVISION LEVEL
G

MICROCIRCUIT, DIGITAL, CMOS, 8 X 8 MULTIPLIER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88739**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88739	01	Q	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Multiply time
01	TMC208KV	Two's complement 8 x 8 multiplier	70 ns
02	TMC208KV1	Two's complement 8 x 8 multiplier	50 ns
03	TMC28KUV	Unsigned magnitude 8 x 8 multiplier	70 ns
04	TMC28KUV1	Unsigned magnitude 8 x 8 multiplier	50 ns
05	LMU0860	Two's complement 8 x 8 multiplier	60 ns
06	LMU0845	Two's complement 8 x 8 multiplier	45 ns
07	LMU8U60	Unsigned magnitude 8 x 8 multiplier	60 ns
08	LMU8U45	Unsigned magnitude 8 x 8 multiplier	45 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
X	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{DD}) ..... -0.5 V dc to +7.0 V dc
DC voltage applied to outputs:
  Devices 01, 02, 03, 04 ..... -0.5 V dc to V_{DD} +0.5 V dc
  Devices 05, 06, 07, 08 ..... -3.0 V dc to +7.0 V dc
DC input voltage:
  Devices 01, 02, 03, 04 ..... -0.5 V dc to V_{DD} +0.5 V dc
  Devices 05, 06, 07, 08 ..... -3.0 V dc to +7.0 V dc
Maximum power dissipation (P_D) ..... 550 mW 1/
Lead temperature (soldering 10 seconds) ..... 300°C
Junction temperature (T_J) ..... 175°C
Thermal resistance, junction to case (θ_{JC}) ..... See MIL-STD-1835
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	4.5 V dc to 5.5 V dc
Output high current (I_{OH})	-2.0 mA maximum
Output low current (I_{OL}):	
Devices 01, 02, 03, 04	4.0 mA maximum
Devices 05, 06, 07, 08	8.0 mA maximum
Input high voltage (V_{IH})	2.0 V minimum
Input low voltage (V_{IL})	0.8 V maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Input/output data format. The input/output data format shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}	V_{DD} = 5.5 V	1, 2, 3	01,02 03,04	2.0 3/		V
				05,06 07,08	2.0		
Input low voltage	V_{IL}	V_{DD} = 5.5 V	1, 2, 3	01,02 03,04		0.8 3/	V
				05,06 07,08		0.8	
High level output voltage	V_{OH}	V_{DD} = 4.5 V, I_{OH} = -2.0 mA	1, 2, 3	01,02 03,04	2.4		V
				05,06 07,08	2.4		
Low level output voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 4.0 mA	1, 2, 3	01,02 03,04		0.4	V
		I_{OL} = 8.0 mA		05,06 07,08		0.5	
Input low current	I_{IL}	V_{DD} = 5.5 V V_{IN} = 0.0 V	1, 2, 3	01,02 03,04		-10	µA
				05,06 07,08		-20	
Input high current	I_{IH}	V_{DD} = 5.5 V $V_{IN} = V_{DD}$	1, 2, 3	01,02 03,04		+10	µA
				05,06 07,08		+20	
Output leakage current, low	I_{OZL}	V_{DD} = 5.5 V V_{IN} = 0.0 V	1, 2, 3	01,02 03,04		-40	µA
				05,06 07,08		-20	
Output leakage current, high	I_{OZH}	V_{DD} = 5.5 V $V_{IN} = V_{DD}$	1, 2, 3	01,02 03,04		+40	µA
				05,06 07,08		+20	
Output short circuit current 2/ 3/	I_{OS}	V_{DD} = 5.5 V	1, 2, 3	01,02 03,04		-100	mA
				05,06 07,08		-125	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Supply current, quiescent	I_{DDQ}	V_{DD} = 5.5 V	V_{IN} = 0.0 V	1, 2, 3	01,02 03,04		5.0	mA
			4/		05,06 07,08		1.0	
Supply current, dynamic	I_{DDU}	V_{DD} = 5.5 V, TRIM, TRIL = 5.0 V, f = 2 MHz		1, 2, 3	01,02 03,04		10	mA
		V_{DD} = 5.5 V, TRIM, TRIL = 5.0 V, f = 20 MHz 3/			01,02 03,04		100	
	I_{DD}	V_{DD} = 5.5 V, TRIM, TRIL = 5.0 V, f = 5 MHz		1, 2, 3	05,06 07,08		24	mA
Input capacitance	C_{IN}	f = 1.0 MHz T_C = 25°C See 4.3.1c		4	All		10	pF
Output capacitance	C_{OUT}			4	All		10	pF
Functional testing 5/		V_{DD} = 4.5 V to 5.5 V See 4.3.1d		7, 8	All			
Multiply time	t_{MPY}	See figure 4 5/ V_{DD} = 4.5 V C_L = 20 pF minimum		9, 10, 11	01,03		70	ns
				10	02,04		50	
				9, 10, 11	05,07		60	
				9, 10, 11	06,08		45	
Output delay	t_D			9, 10, 11	01,03		45	ns
				10	02,04		30	
				9, 10, 11	05,06 07,08		22	
Input setup time	t_S			9, 10, 11	01,03	30		ns
				10	02,04	25		
				9, 10, 11	05,06 07,08	15		
Input hold time 3/	t_H			9, 10, 11	All	0		ns
Clock pulse width, high	t_{PWH}			9, 10, 11	01,02 03,04	15		ns
				9, 10, 11	05,07	20		
				9, 10, 11	06,08	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock pulse width, low	t_{PWL}	See figure 4. 5/ V_{DD} = 4.5 V C_L = 20 pF minimum 3/	9, 10, 11	01,02 03,04	15		ns
			9, 10, 11	05,07	20		
			9, 10, 11	06,08	15		
Three-state output enable time	t_{ENA}	See figure 4. 5/ V_{DD} = 4.5 V C_L = 20 pF minimum	9, 10, 11	01,03		45	ns
			10	02,04		25	
			9, 10, 11	05,06 07,08		24	
Three-state output disable time	t_{DIS}		9, 10, 11	01,03		45	ns
			10	02,04		25	
			9, 10, 11	05,06 07,08		22	

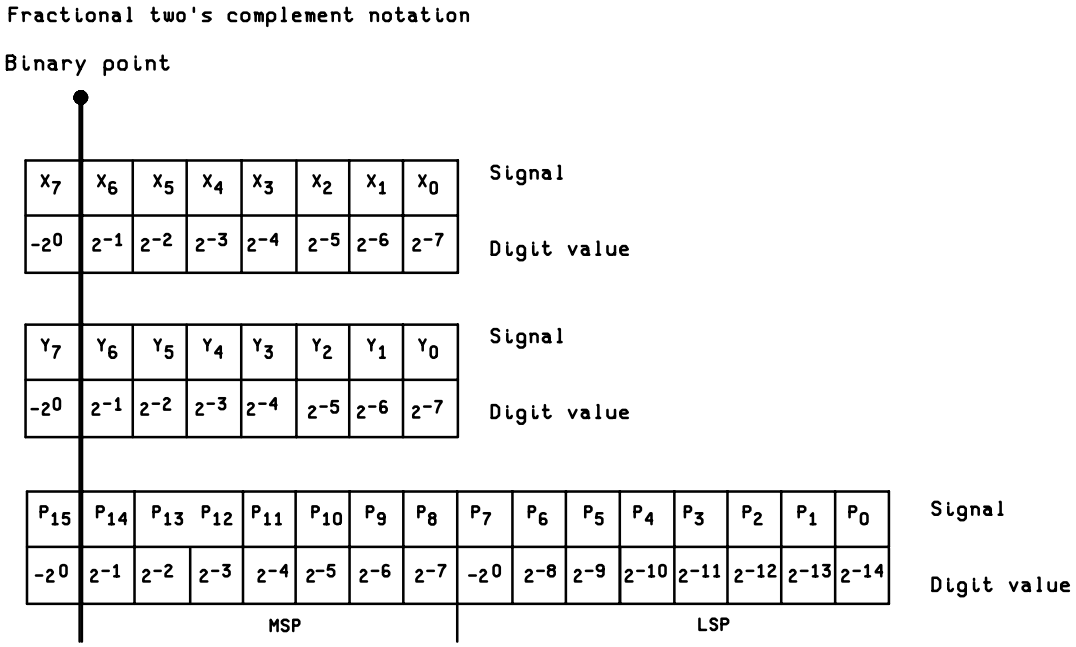
1/ Unless otherwise specified, all testing shall be conducted under worst case conditions.
2/ One output to ground, 1 second duration maximum, output high.
3/ Guaranteed, if not tested, to the specified limits.
4/ Tested with all inputs within 0.1 V of V_{DD} or ground, no load.
5/ All transitions are measured at a 1.5 V level except t_{DIS} or t_{ENA}.

Device types	All		
Case outline	Q		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P_{10}	21	X_6
2	P_9	22	X_7
3	P_8	23	CLK X
4	CLK P	24	CLK Y
5	TRIM	25	RND
6	TRIL	26	Y_0
7	P_7	27	Y_1
8	P_6	28	Y_2
9	P_5	29	Y_3
10	P_4	30	V_{DD}
11	P_3	31	Y_4
12	P_2	32	GND
13	P_1	33	Y_5
14	P_0	34	Y_6
15	X_0	35	Y_7
16	X_1	36	P_{15}
17	X_2	37	P_{14}
18	X_3	38	P_{13}
19	X_4	39	P_{12}
20	X_5	40	P_{11}

Device types	All		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P_{10}	23	X_6
2	P_9	24	X_7
3	P_8	25	CLK X
4	CLK P	26	CLK Y
5	TRIM	27	RND
6	NC	28	NC
7	TRIL	29	Y_0
8	P_7	30	Y_1
9	P_6	31	Y_2
10	P_5	32	Y_3
11	P_4	33	V_{DD}
12	P_3	34	Y_4
13	P_2	35	GND
14	P_1	36	Y_5
15	P_0	37	Y_6
16	X_0	38	Y_7
17	NC	39	NC
18	X_1	40	P_{15}
19	X_2	41	P_{14}
20	X_3	42	P_{13}
21	X_4	43	P_{12}
22	X_5	44	P_{11}

FIGURE 1. Terminal connections.

Device types 01, 02, 05, and 06



Device types 01, 02, 05, and 06

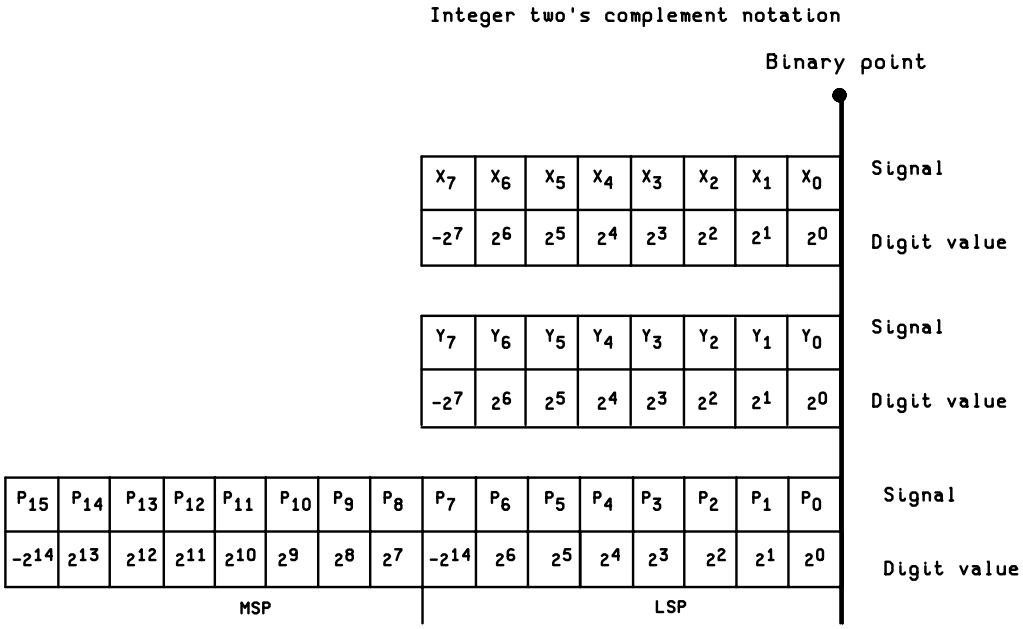
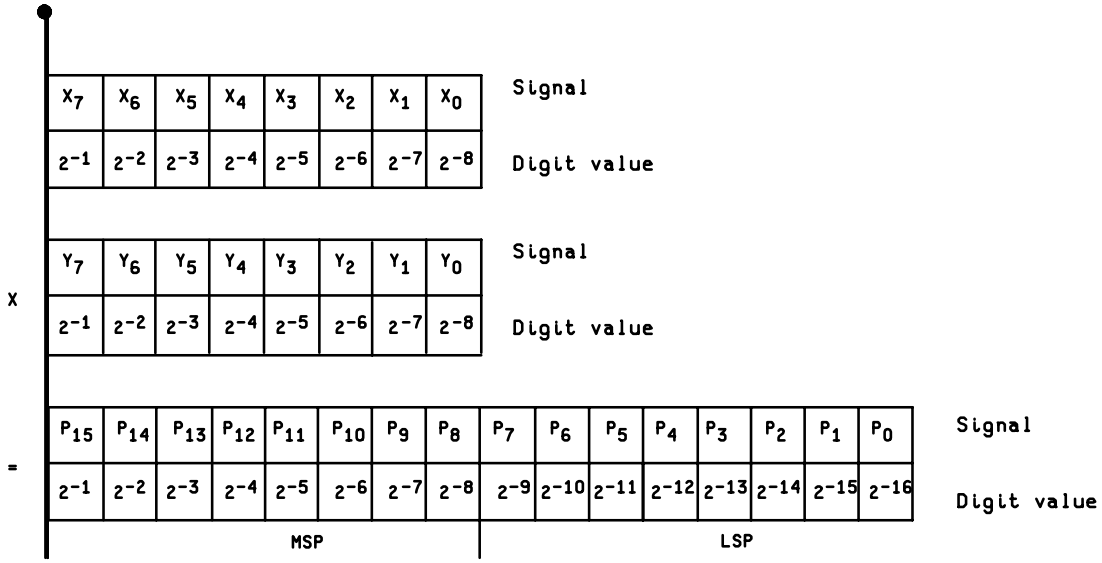


FIGURE 2. Input/output data format.

Device types 03, 04, 07, and 08

Fractional unsigned magnitude notation



Device types 03, 04, 07, and 08

Integer unsigned magnitude notation

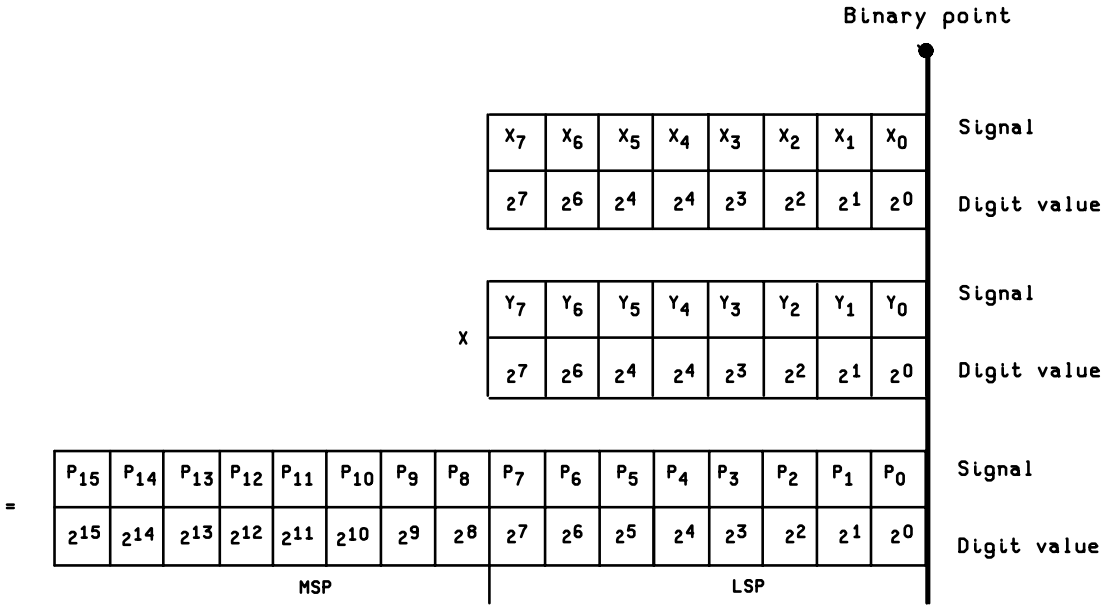
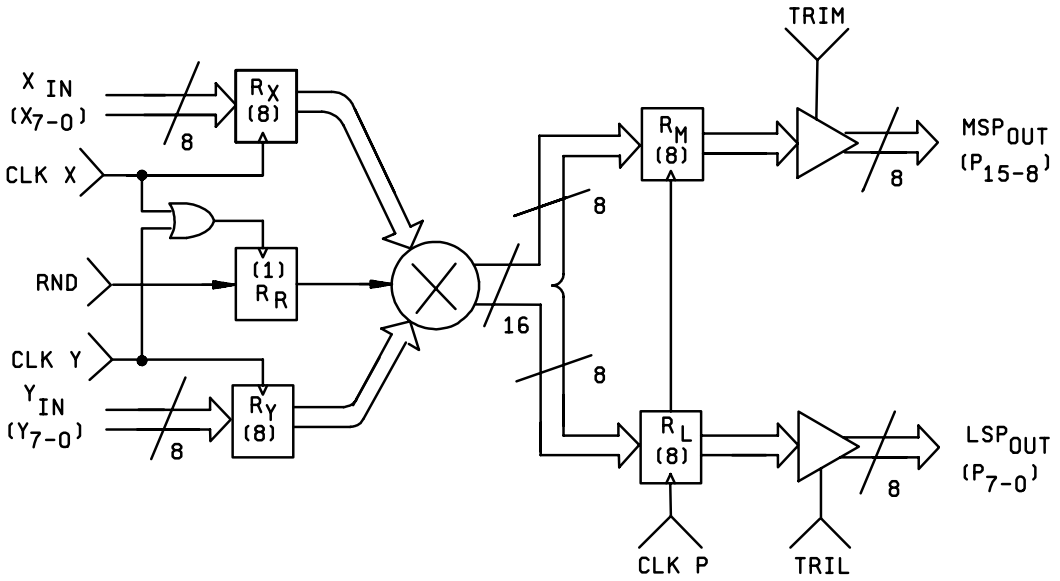


FIGURE 2. Input/output data format - Continued.

Device types 01, 02, 05, and 06



Device types 03, 04, 07, and 08

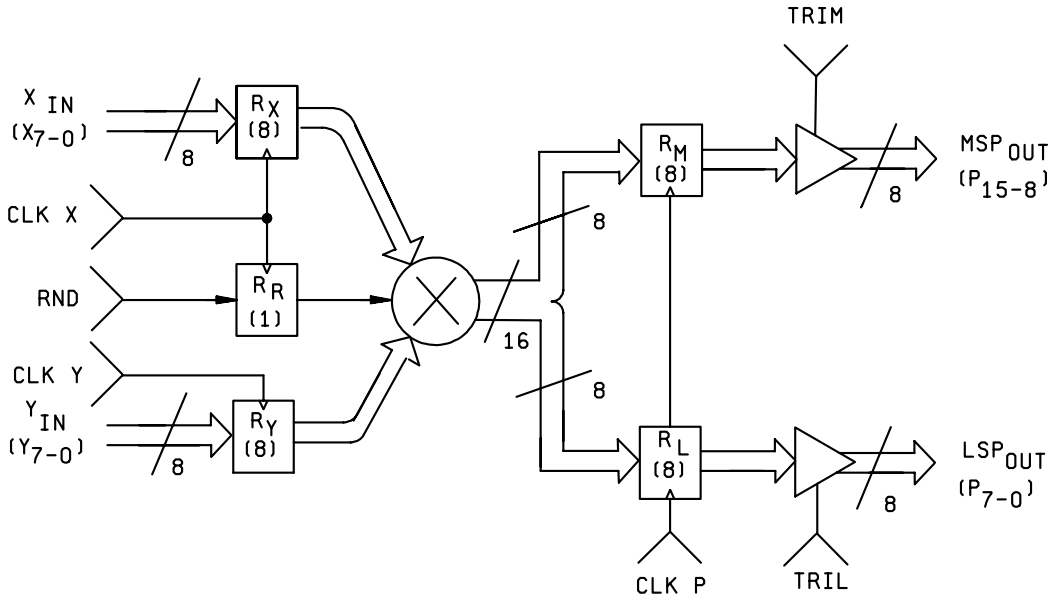


FIGURE 3. Block diagram.

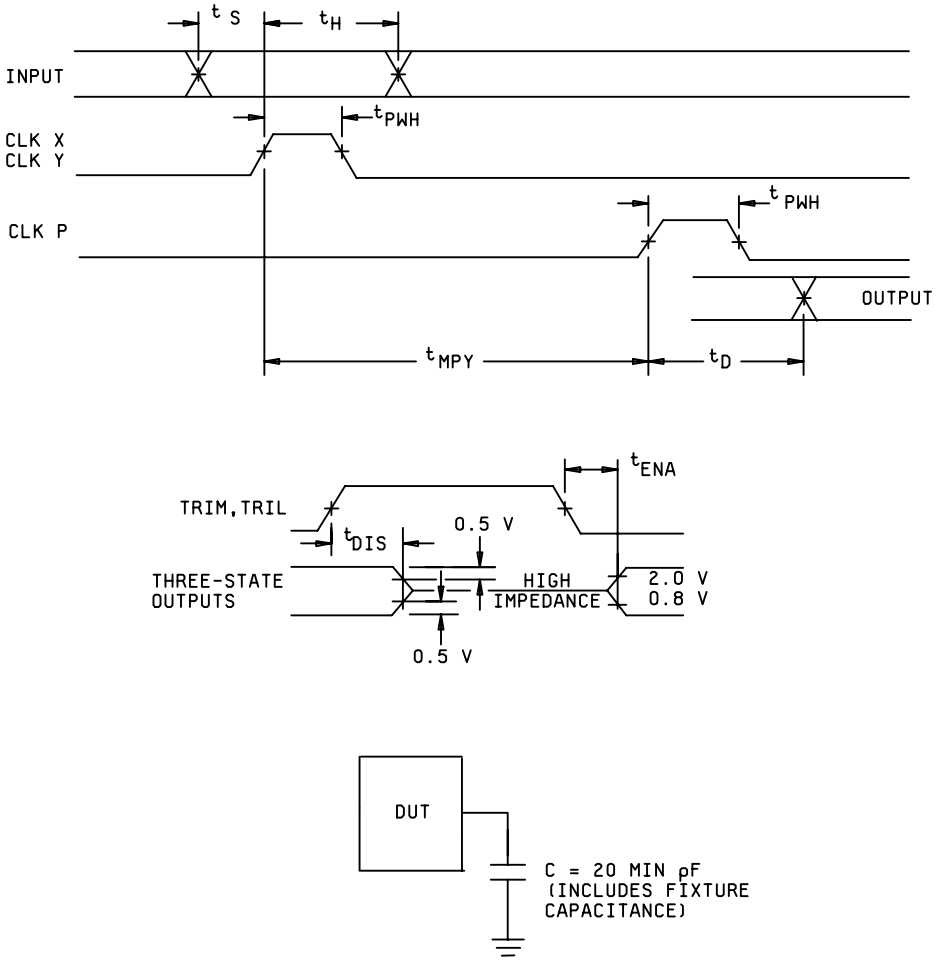


FIGURE 4. Test circuit and switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 7, 9

* PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall include verification of the functionality of the device.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Pin descriptions. See table III.

TABLE III. Pin descriptions.

Pin	Description
V_{DD}, GND	The devices operate from a single +5.0 V supply. All power and ground lines must be connected.
X_{7-0} Y_{7-0}	Devices 01, 02, 05, and 06 have two 8-bit two's complement data inputs labeled X and Y. Devices 03, 04, 07, and 08 have two 8-bit unsigned magnitude data inputs labeled X and Y. The most significant bits (MSB's) X_7 and Y_7, carry the sign information for the two's complement notation in devices 01, 02, 05, and 06. The remaining bits are X_{6-0} and Y_{6-0} with X_0 and Y_0 the LSB's. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown on figure 2.
P_{15-0}	Devices 01, 02, 05, and 06 have a 16-bit two's complement output which is the product of the two input X and Y values. Devices 03, 04, 07, and 08 have a 16-bit unsigned magnitude output which is the product of the two input X and Y values. This output is divided into two 8-bit output words, the MSP and LSP. The MSB of both the MSP and LSP is the sign bit in devices 01, 02, 05, and06. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown on figure 2. Note that since +1 cannot be exactly represented in fractional two's complement notation, some provision for handling the case (-1)∗(-1) must be made. Devices 01, 02, 05, and 06 output a –1 in this case. As a result, external error handling provisions may be required.
CLK X, CLK Y, CLK P	These devices have three clock lines, one for each input register (CLK X and CLK Y) and one for the product register (CLK P). Data present at the inputs of these registers are loaded into the registers on the rising edge of the appropriate clock. In devices 01, 02, 05, and 06, the RND input is registered and clocked in on the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally high clock signals are used. Problems with loading this control signal can be avoided by the use of normally low clocks. In devices 03, 04, 07, and 08, the RND input is registered and clocked in on the rising edge of CLK X.
TRIM, TRIL	TRIM and TRIL are the three-state enable lines for the MSP and LSP. The output driver is in the high impedance state when TRIM or TRIL is high, and enabled when low. TRIM and TRIL are not registered.
RND	When RND (round) is high, one is added to the MSB of the LSP. A one will be added to the P_6 bit in devices 01, 02, 05, and 06, or the P_7 bit in devices 03, 04, 07, and 08. Note that rounding always occurs in the positive direction. In some applications, this may introduce a systematic bias. The RND input is registered and used when a rounded 8-bit product is desired.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-08-15

Approved sources of supply for SMD 5962-88739 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8873901QA	0C7V7	TMC208K
5962-8873901XA	0C7V7	TMC208KC2V
5962-8873902QA	0C7V7	TMC208K
5962-8873902XA	0C7V7	TMC208KC2V1
5962-8873903QA	0C7V7	TMC208KU
5962-8873903XA	0C7V7	TMC208KU
5962-8873904QA	0C7V7	TMC208KU
5962-8873904XA	0C7V7	TMC208KU
5962-8873905QA	0C7V7	TMC208K
5962-8873905XA	0C7V7	TMC208K
5962-8873906QA	0C7V7	TMC208K
5962-8873906XA	0C7V7	TMC208K
5962-8873907QA	0C7V7	TMC208KU
5962-8873907XA	0C7V7	TMC208KU
5962-8873908QA	0C7V7	TMC208KU
5962-8873908XA	0C7V7	TMC208KU

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051