1GB – 2x64Mx64 DDR SDRAM, UNBUFFERED, FBGA

FEATURES

- Fast data transfer rate: PC-2100, PC-2700 and PC3200
- Clock speeds of 133 MHz, 166 MHz and 200MHz
- Supports ECC error detection and correction
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 3 and 4 (clock)
- Programmable Burst Length (2, 4 or 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect (SPD) with EEPROM
- $V_{CC} = V_{CCQ}$ = +2.6V ±0.1V (200MHz)
- $V_{CC} = V_{CCQ}$ = +2.5V ±0.2V (133 and 166MHz)
- Gold edge contacts
- Dual Rank
- JEDEC standard 200 pin, small-outline, SO-DIMM package
  - PCB height option:
    D4: 31.75 mm (1.25") TYP

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

DESCRIPTION

The W3EG264M64EFSU is a 2x64Mx64 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM components. The module consists of sixteen 64Mx8 DDR SDRAMs in FBGA packages mounted on a 200 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

OPERATING FREQUENCIES

	DDR400@CL=3	DDR333@CL=2.5	DDR266@CL=2	DDR266@CL=2.5
Clock Speed	200MHz	166MHz	133MHz	133MHz
CL-t_{RCD}-t_{RP}	3-3-3	2.5-3-3	2-2-2	2.5-3-3

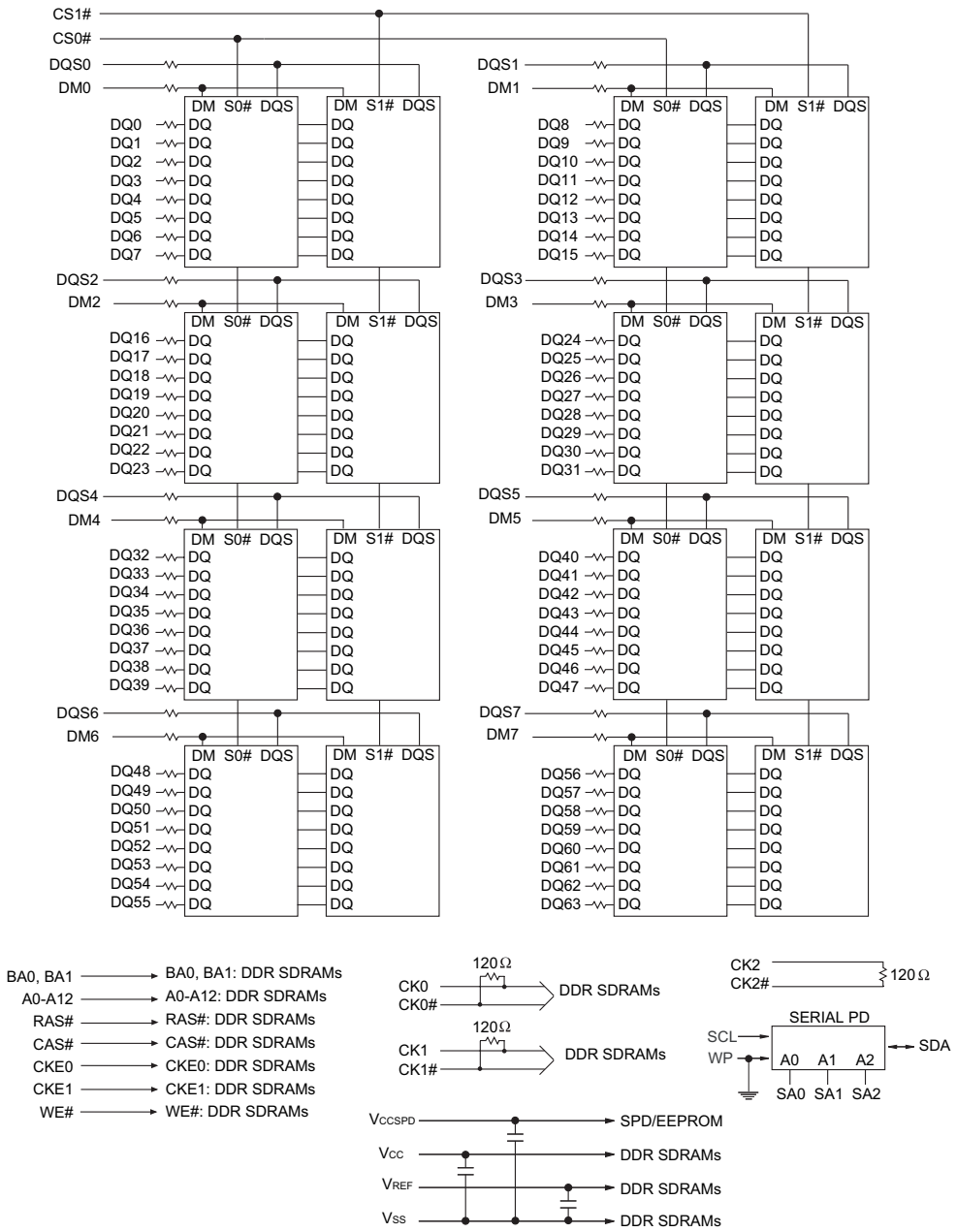
PIN CONFIGURATION

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	V_{REF}	51	V_{SS}	101	A9	151	DQ42
2	V_{REF}	52	V_{SS}	102	A8	152	DQ46
3	V_{SS}	53	DQ19	103	V_{SS}	153	DQ43
4	V_{SS}	54	DQ23	104	V_{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V_{CC}
6	DQ4	56	DQ28	106	A6	156	V_{CC}
7	DQ1	57	V_{CC}	107	A5	157	V_{CC}
8	DQ5	58	V_{CC}	108	A4	158	CK1#
9	V_{CC}	59	DQ25	109	A3	159	V_{SS}
10	V_{CC}	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	V_{SS}
12	DM0	62	DM3	112	A0	162	V_{SS}
13	DQ2	63	V_{SS}	113	V_{CC}	163	DQ48
14	DQ6	64	V_{SS}	114	V_{CC}	164	DQ52
15	V_{SS}	65	DQ26	115	A10	165	DQ49
16	V_{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V_{CC}
18	DQ7	68	DQ31	118	RAS#	168	V_{CC}
19	DQ8	69	V_{CC}	119	WE#	169	DQS6
20	DQ12	70	V_{CC}	120	CAS#	170	DM6
21	V_{CC}	71	DNU	121	CS0#	171	DQ50
22	V_{CC}	72	DNU	122	CS1#	172	DQ54
23	DQ9	73	DNU	123	NC	173	V_{SS}
24	DQ13	74	DNU	124	NC	174	V_{SS}
25	DQS1	75	V_{SS}	125	V_{SS}	175	DQ51
26	DM1	76	V_{SS}	126	V_{SS}	176	DQ55
27	V_{SS}	77	DNU	127	DQ32	177	DQ56
28	V_{SS}	78	DNU	128	DQ36	178	DQ60
29	DQ10	79	DNU	129	DQ33	179	V_{CC}
30	DQ14	80	DNU	130	DQ37	180	V_{CC}
31	DQ11	81	V_{CC}	131	V_{CC}	181	DQ57
32	DQ15	82	V_{CC}	132	V_{CC}	182	DQ61
33	V_{CC}	83	DNU	133	DQS4	183	DQS7
34	V_{CC}	84	DNU	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V_{SS}
36	V_{CC}	86	DNU	136	DQ38	186	V_{SS}
37	CK0#	87	V_{SS}	137	V_{SS}	187	DQ58
38	V_{SS}	88	V_{SS}	138	V_{SS}	188	DQ62
39	V_{SS}	89	DNU	139	DQ35	189	DQ59
40	V_{SS}	90	V_{SS}	140	DQ39	190	DQ63
41	DQ16	91	DNU	141	DQ40	191	V_{CC}
42	DQ20	92	V_{CC}	142	DQ44	192	V_{CC}
43	DQ17	93	V_{CC}	143	V_{CC}	193	SDA
44	DQ21	94	V_{CC}	144	V_{CC}	194	SA0
45	V_{CC}	95	CKE1	145	DQ41	195	SCL
46	V_{CC}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V_{CCSPD}
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	V_{SS}	199	NC
50	DQ22	100	A11	150	V_{SS}	200	V_{SS}

PIN NAMES

Symbol	Description
A0-A12	Address input
BA0, BA1	Bank Address
DQ0-DQ63	Input/Output: Data I/Os, Data bus
CB0-CB7	Input/Output: Check Bits
CK0, CK0# CK1, CK1# CK2, CK2#	Clock Input
CKE0-CKE1	Clock Enable Input
CS0#-CS1#	Chip Select Input
WE#, CAS#, RAS#	Command Input
DQS0-DQS8	Data Strobe
DM0-DM8	Data Write Mask
V_{CC}	Supply: Power Supply: +2.5V ±0.2V
V_{CCSPD}	Supply: Serial EEPROM Positive Power Supply
V_{REF}	Supply: SSTL_2 reference voltage
V_{SS}	Supply: Ground
SCL	Serial Clock
SA0-SA2	Presence Detect Address Input
SDA	Input/Output: Serial Presence-Detect Data
NC	No Connect
DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



Note: 1. All resistor values are 22Ω unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	2.3	2.7	V
I/O Supply Voltage	V_{CCQ}	2.3	2.7	V
I/O Reference Voltage	V_{REF}	0.49 × V_{CCQ}	0.51 × V_{CCQ}	V
I/O Termination Voltage (system)	V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.15	V_{CC} + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3	V_{REF} - 0.15	V
High Current (V_{OUT} = V_{CCQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OH}	-16.8	—	mA
Low Current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OL}	16.8	—	mA

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS
Input/Output Capacitance: DQ, DQS,DM	C_{I0}	12	pF
Input Capacitance: Command and Address	C_{I1}	47	pF
Input Capacitance: CK, CK#,	C_{I2}	25	pF
Input Capacitance: CKE, S#	C_{I3}	25	pF

I_{DD} SPECIFICATIONS AND CONDITIONS

0°C ≤ T_A ≤ +70°C; V_{CC}, V_{CCQ} = +2.5V ±0.2V

DDR400: V_{CC} = V_{CCQ} = +2.6V ±0.2V

PARAMETER/CONDITION	SYM	MAX				UNITS
		DDR400 @CL=3	DDR333 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2.5	
OPERATING CURRENT: One device bank; Active-Precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I_{CC0}	2475	2070	2070	1845	mA
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 4; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle	I_{CC1}	2745	2340	2340	2115	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (MIN); CKE = (LOW)	I_{CC2P}	90	90	90	90	mA
IDLE STANDBY CURRENT: CS# = HIGH; All device banks are idle; t_{CK} = t_{CK} (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM	I_{CC2F}	990	810	810	720	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; t_{CK} = t_{CK} (MIN); CKE = LOW	I_{CC3P}	810	630	630	540	mA
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank active; t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I_{CC3N}	1080	900	900	810	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	I_{CC4R}	2790	2385	2385	2115	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I_{CC4W}	2790	2295	2295	2025	mA
AUTO REFRESH BURST CURRENT: t_{REFC} = t_{RFC} (MIN)	I_{CC5}	4185	3510	3510	3330	mA
SELF REFRESH CURRENT: CKE ≤ 0.2V	I_{CC6}	90	90	90	90	mA
OPERATING CURRENT: Four device bank interleaving READs (Burst = 4) with auto precharge, t_{RC} = minimum t_{RC} allowed; t_{CK} = t_{CK} (MIN); Address and control inputs change only during Active READ, or WRITE commands	I_{CC7}	5130	4545	4545	3960	mA

Note: I_{CC} specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

$0°C \le T_A \le +70°C$

AC CHARACTERISTICS		SYMBOL	403		335		262		265		UNITS	NOTES
PARAMETER			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Access window of DQs from CK/CK#		t_{AC}	-0.65	+0.65	-0.70	+0.70	-0.75	+0.75	-0.75	0.75	ns	
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	26
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	26
Clock cycle time	CL = 3	$t_{CK\ (3)}$	5	10							ns	39, 44
	CL = 2.5	$t_{CK\ (2.5)}$			6	12	7.5	13	7.5	13	ns	39, 44
	CL = 2	$t_{CK\ (2)}$			7.5	12	7.5	13	7.5/10	13	ns	39, 44
DQ and DM input hold time relative to DQS		t_{DH}	0.40		0.45		0.5		0.5		ns	23, 27
DQ and DM input setup time relative to DQS		t_{DS}	0.40		0.45		0.5		0.5		ns	23, 27
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75		1.75		1.75		1.75		ns	27
Access window of DQS from CK/CK#		t_{DQSCK}	-0.55	+0.55	-0.60	+0.60	-0.75	+0.75	-0.75	+0.75	ns	
DQS input high pulse width		t_{DQSH}	0.35		0.35		0.35		0.35		t_{CK}	
DQS input low pulse width		t_{DQSL}	0.35		0.35		0.35		0.35		t_{CK}	
DQS - DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.4		0.4		0.5		0.5	ns	22, 23
Write command to first DQS latching transition		t_{DQSS}	0.72	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS falling edge to CK rising - setup time		t_{DSS}	0.20		0.20		0.20		0.2		t_{CK}	
DQS falling edge from CK rising - hold time		t_{DSH}	0.20		0.20		0.20		0.2		t_{CK}	
Half clock period		t_{HP}	t_{CH},t_{CL}		t_{CH},t_{CL}		t_{CH},t_{CL}		t_{CH}, t_{CL}		ns	30
Data-out high-impedance window from CK/CK#		t_{HZ}	-0.65	+0.65	-0.70	+0.70	-0.75	+0.75	-0.75	+0.75	ns	16, 36
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.65	+0.65	-0.70		-0.75		-0.75		ns	16, 36
Address and control input hold time (fast slew rate)		t_{IHF}	0.60		0.75		0.90		0.90		ns	12
Address and control input setup time (fast slew rate)		t_{ISF}	0.60		0.75		0.90		0.90		ns	12
Address and control input hold time (slow slew rate)		t_{IHS}	0.7		0.8		1		1		ns	12

AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

Continued on next page

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Con't)

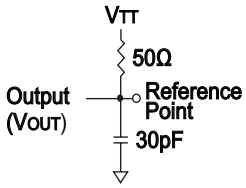
0°C < T_A <+70°C

AC CHARACTERISTICS		403		335		262		265		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Address and control input setup time (slow slew rate)	t_{ISS}	0.8		0.8		1		1	ns	12	
Address and Control input pulse width (for each input)	t_{IPW}	2.2		2.2		2.2		2.2		ns	
LOAD MODE REGISTER command cycle time	t_{MRD}	10		12		15		15		ns	
DQ - DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ns	22, 23
Data hold skew factor	t_{QHS}		0.50		0.50		0.75		0.75	ns	
ACTIVE to PRECHARGE command	t_{RAS}	40	70,000	42	70,000	40	120,000	40	120,000	ns	30, 47
ACTIVE to READ with Auto precharge command	t_{RAP}	15		18		15		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period	t_{RC}	55		60		60		65		ns	
AUTO REFRESH command period	t_{RFC}	70		72		75		78		ns	42
ACTIVE to READ or WRITE delay	t_{RCD}	15		18		15		20		ns	
PRECHARGE command period	t_{RP}	15		18		15		20		ns	
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	37
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	37
ACTIVE bank *a* to ACTIVE bank *b* command	t_{RRD}	10		12		15		15		ns	
DQS write preamble	t_{WPRE}	0.25		0.25		0.25		0.25		t_{CK}	
DQS write preamble setup time	t_{WPRES}	0		0		0		0		ns	18, 19
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	17
Write recovery time	t_{WR}	15		15		15		15		ns	
Internal WRITE to READ command delay	t_{WTR}	2		1		1		1		t_{CK}	
Data valid output window		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns	22
REFRESH to REFRESH command interval	t_{REFC}		70.3		70.3		70.3		70.3	µs	21
Average periodic refresh interval	t_{REFI}		7.8		7.8		7.8		7.8	µs	21
Terminating voltage delay to V_{CC}	t_{VTD}	0		0		0		0		ns	
Exit SELF REFRESH to non-READ command	t_{XSNR}	75		75		75		75	ns		
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		200		200		t_{CK}	

AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

Notes

1. All voltages referenced to V_{SS}
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at normal reference / supply voltage levels, but the related specifications and device operations are guaranteed for the full voltage range specified.
3. Outputs are measured with equivalent load:



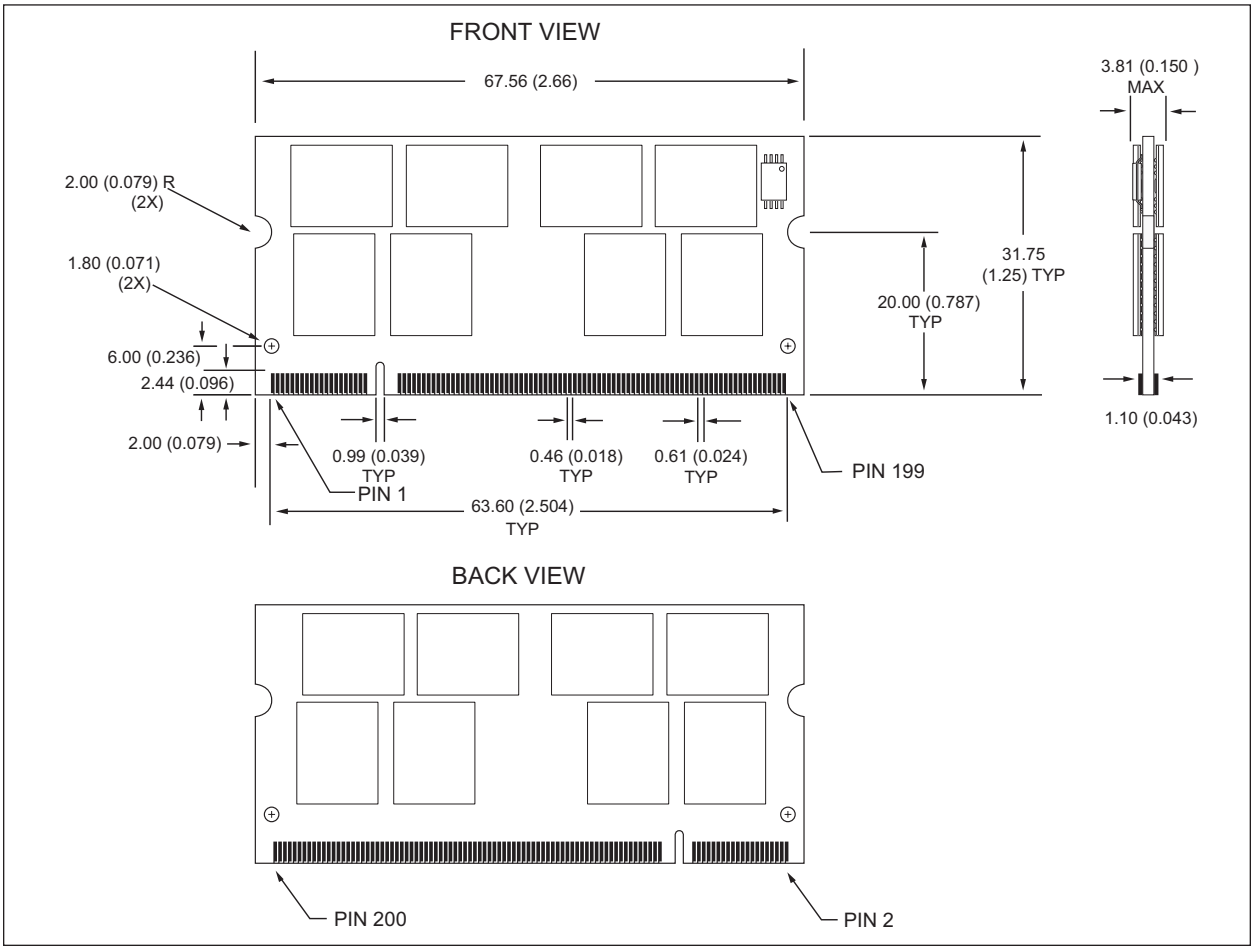
4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).
5. The AC and DC input level specifications are defined in the SSTL_2 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [high] level).
6. For slew rates less than 1V/ns and greater than or equal to 0.5V/ns. If the slew rate is less than 0.5V/ns, timing must be derated: t_{IS} has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. t_{IH} has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain. For 403 and 335, slew rates must be greater than or equal to 0.5V/ns.
7. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE □ 0.3 x V_{CCQ} is recognized as LOW.
8. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) and begins driving (LZ).
9. The intent of the “Don’t Care” state after completion of the postamble is the DQS-driven signal should either be HIGH, LOW, or high-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above V_{IHDC} (MIN) then it must not transition LOW (below V_{IHDC}) prior to t_{DQSH} (MIN).
10. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
11. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be high during this time, depending on t_{DQSS}.
12. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
13. The valid data window is derived by achieving other specifications - t_{HP} ($t_{CK/2}$), t_{DQSQ}, and t_{QH} (t_{QH} = t_{HP} - t_{QHS}). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycled variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
14. Referenced to each output group: x8 = DQS with DQ0-DQ7.
15. READs and WRITEs with auto precharge are not allowed to be issued until t_{RAS} (MIN) can be satisfied prior to the internal precharge command being issued.
16. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
17. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to t_{DS} and t_{DH} for each 100mV/ns reduction in slew rate. If slew rates exceed 4V/ns, functionality is uncertain.
18. t_{HP} min is the lesser of t_{CL} min and t_{CH} min actually applied to the device CK and CK# inputs, collectively during bank active.
19. t_{HZ} (MAX) will prevail over the t_{DQSCK} (MAX) + t_{RPST} (MAX) condition. t_{LZ} (MIN) will prevail over t_{DQSCK} (MIN) + PRE (MAX) condition.
20. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
21. CKE must be active (High) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until t_{RFC} has been satisfied.
22. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles (before READ commands).

ORDERING INFORMATION FOR D4

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
W3EG264M64EFSU403D4xxx	200MHz/400Mbps	3	3	3	31.75 (1.25") TYP
W3EG264M64EFSU335D4xxx	166MHz/333Mbps	2.5	3	3	31.75 (1.25") TYP
W3EG264M64EFSU262D4xxx	133MHz/266Mbps	2	2	2	31.75 (1.25") TYP
W3EG264M64EFSU265D4xxx	133MHz/266Mbps	2.5	3	3	31.75 (1.25") TYP

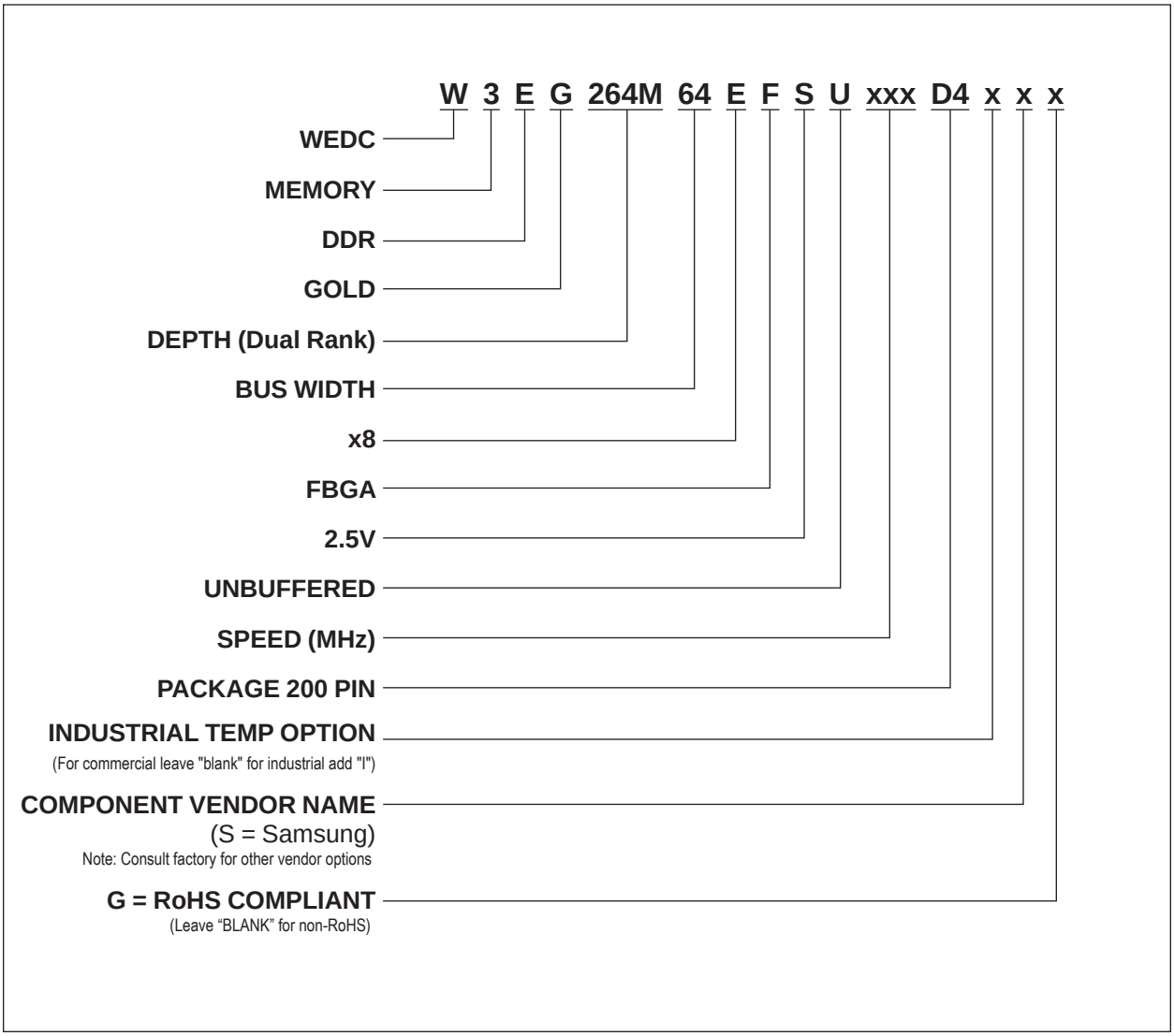
NOTES:
- For part numbering interpretation, please see "part number guide" on page 10.

200-PIN DDR2 SODIMM DIMENSIONS



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

1GB - 2x64Mx64 DDR SDRAM, UNBUFFERED, FBGA

DRAM DIE OPTIONS:

- SAMSUNG: C-Die
- MICRON: F-Die
- QIMONDA: C-Die

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	8-05	Advanced
Rev 1	1.0 Moved to advanced to preliminary 1.1 Updated vendor source information 1.2 Updated part numbering 1.3 Added “DRAM Die Options”	5-07	Advanced