1.0 SCOPE

This specification covers the detail requirements for a buffered 8-bit digital-to-analog converter designed specifically for 8-bit bus oriented systems.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace spec control drawings.

1.2 Part Number. The complete part numbers per Table I of this specification follow:

Device	Part Number	Package
A	DAC-888AX/883	X
B	DAC-888BX/883	X

1.2.3 Case Outline.

Letter	Case Outline (Lead finish per MIL-M-38510)
X	18-lead ceramic dual-in-line package (CERDIP)

1.3 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
V+ Supply to Analog Ground ..... 0 to +18V
V- Supply to Analog Ground ..... 0 to -18V
Analog Current Outputs ..... -5mA
V+ Supply to V- Supply 18.1V
Logic Inputs ..... 0V to 5.5V
Reference Inputs (V_{10} to V_{11}) ..... V- to V+
Reference Input Differential Voltage (V_{10} to V_{11}) ..... ±15V
Power Dissipation 300mW
Derate Above 100°C ..... 10mW/°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C
Reference Input Current 5mA

1.5 Thermal Characteristics:

Thermal Resistance, CERDIP (X) package:
Junction-to-Case (Θ_{JC}) = 35°C/W MAX
Junction-to-Ambient (Θ_{JA}) = 120°C/W MAX

January 1988

TABLE 1

V+ = +5V; V- = -12V; I_{REF} = 2mA; -55°C ≤ T_A ≤ +125°C unless otherwise specified
Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Characteristics	Symbol	Special Conditions	DAC-888/883 LIMITS A Min	LIMITS A Max	LIMITS B Min	LIMITS B Max	Units
Monotonicity			8	–	8	–	Bits
Nonlinearity	NL		–	±0.1	–	±0.19	%FS
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < ±1/2 LSB	-5	+5	-5	+5	V
Full Range Current	I_{FR}	V_{REF} = 10.000V R_{11}, R_{10} = 5.000kΩ	1.94	2.04	1.94	2.04	mA
Full Range Symmetry	I_{FRS}	I_{FR14} - I_{FR13}	–	±8	–	±8	µA
Zero-Scale Current	I_{ZS}		–	±2	–	±2	µA
Reference Bias Current	I_B		–	-3	–	-3	µA
Power Supply Sensitivity	PSS_{IFS+}	V+ = 4.5V to 5.5V; V- = -12V I_{REF} = 2mA	–	±0.01	–	±0.01	$\frac{\%\Delta I_{FS}}{\%\Delta V+}$
	PSS_{IFS-}	V- = -10.8V to -13.2V; V+ = 5V I_{REF} = 1mA	–	±0.01	–	±0.01	$\frac{\%\Delta I_{FS}}{\%\Delta V}$
Power Supply Current	I+		–	16	–	16	mA
	I-		–	-9	–	-9	mA
Power Dissipation (Note 1)	P_d		–	190	–	190	mW
Output Current Range	I_{FSR}	I_{REF} = 3mA	2.1	–	2.1	–	mA
Logic Input Levels "0" "1"	V_{IL}	$\overline{I_{FR}}$ within spec	–	0.8	–	0.8	V
	V_{IH}	I_{FR} within spec	2	–	2	–	V

TABLE 1 (Continued)

V+ = +5V; V- = -12V; I_{REF} = 2mA; -55°C ≤ T_A ≤ +125°C unless otherwise specified
Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Characteristics	Symbol	Special Conditions	DAC-888/883 LIMITS A Min	LIMITS A Max	LIMITS B Min	LIMITS B Max	Units
Output Current Range	I_{FSR}	I_{REF} = 3mA	2.1	–	2.1	–	mA
Logic Input Levels "0" "1"	V_{IL}	$\overline{I_{FR}}$ within spec	–	0.8	–	0.8	V
	V_{IH}	I_{FR} within spec	2	–	2	–	V
Logic Input Current	I_{IL}	V_{IN} = 0V	–	-10	–	-10	µA
	I_{IH}	V_{IN} = 5.25V	–	1	–	1	µA

NOTES:
1. Power dissipation (P_d) limits are guaranteed by power supply current (I±) testing.

TABLE 2

DAC-888/883

Electrical Test Requirements
For Class B Devices

MIL-STD-883 Test Requirements	Subgroups (see Table 3)
Interim Electrical Parameters (pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3

* PDA applies to Subgroup 1 only.
No other Subgroups are included in PDA.

TABLE 3

Group A Inspection

V+ = +5V; V- = -12V; I_{REF} = 2mA unless otherwise specified
Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Subgroup	Symbol	Special Conditions	DAC-888/883 LIMITS A Min	LIMITS A Max	LIMITS B Min	LIMITS B Max	Units
Subgroup 1	Monotonicity		8	–	8	–	Bits
T_A = +25C	NL		–	±0.1	–	±0.19	%FS
	V_{OC}	Full-Scale Current Change < ±1/2 LSB	-5	+5	-5	+5	V
	I_{FR}	V_{REF} = 10.000V R_{11}, R_{10} = 5.000kΩ	1.94	2.04	1.94	2.04	mA
	I_{ZS}		–	±2	–	±2	µA
	PSS_{IFS+}	V+ = 4.5V, 5.5V; V- = -12V I_{REF} = 2mA	–	±0.01	–	±0.01	$\frac{\%\Delta I_{FS}}{\%\Delta V+}$
	PSS_{IFS-}	V- = -10.8V, -13.2V; V+ = 5V I_{REF} = 1mA	–	±0.01	–	±0.01	$\frac{\%\Delta I_{FS}}{\%\Delta V-}$
	I+		–	16	–	16	mA
	I-		-9	–	-9	–	mA
	V_{IL}	$\overline{I_{FR}}$ within spec	–	0.8	–	0.8	V
	V_{IH}	I_{FR} within spec	2	–	2	–	V
	I_{IL}	V_{IN} = 0V	–	-10	–	-10	µA
	I_{IH}	V_{IN} = 5.25V	–	1	–	1	µA
	I_{FSR}	I_{REF} = 3mA	2.1	–	2.1	–	mA
	I_{FRS}	I_{FR14} - I_{FR13}	–	±8	–	±8	µA
	I_B		-3	–	-3	–	µA

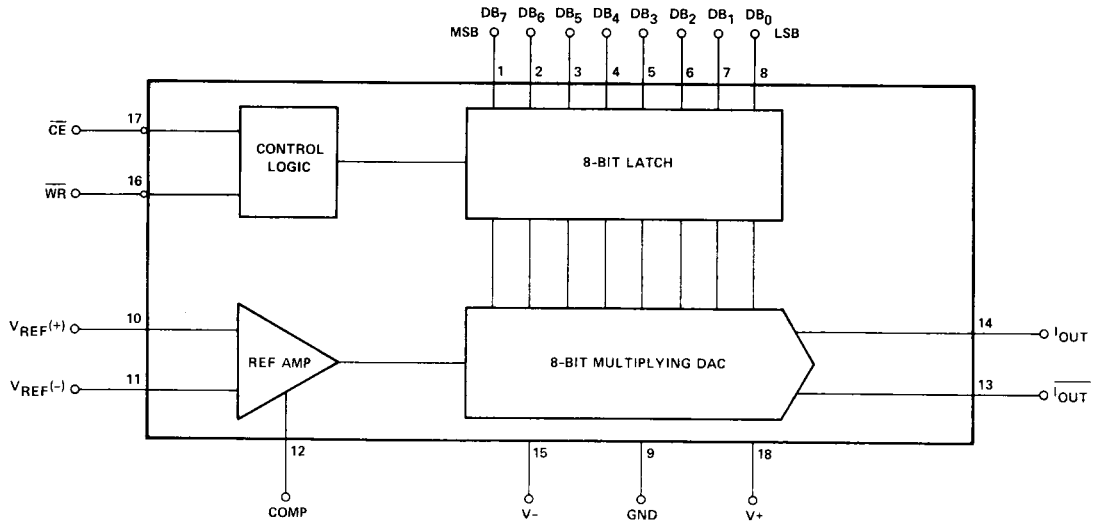
TABLE 3

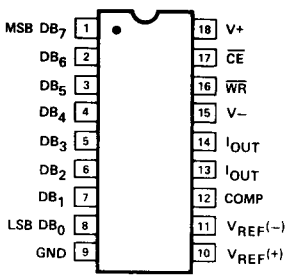
Group A Inspection (Continued)

V+ = +5V; V- = -12V; I_{REF} = 2mA unless otherwise specified
Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-888/883				
			LIMITS A		LIMITS B		
Subgroup	**Symbol**	**Special Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
Subgroup 2 T_A = +125C		All Tests, Limits and Conditions are the same as for Subgroup 1.					
Subgroup 3 T_A = -55°C		All Tests, Limits and Conditions are the same as for Subgroup 2.					

3.2.1 Functional Diagram and Pin Connections.

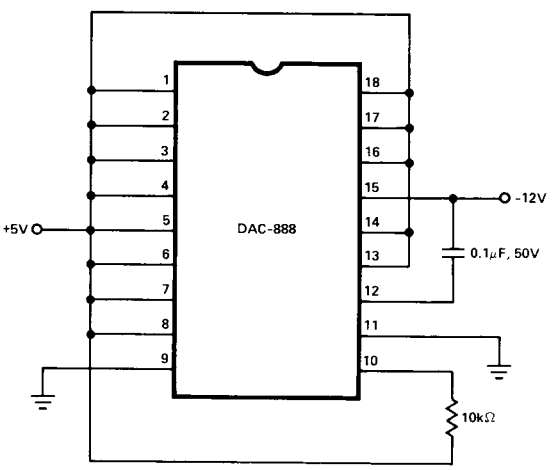




18-PIN HERMETIC DUAL-IN-LINE PACKAGE (X-Suffix)

3.2.4 Microcircuit Group Assignment. This microcircuit is covered by microcircuit group 56.

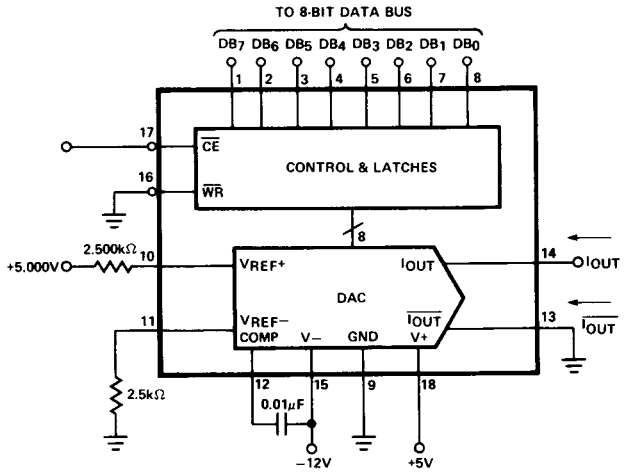
4.2 Life Test/Burn-In Circuit.

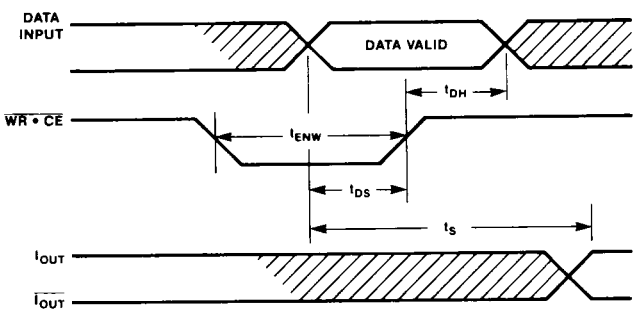


DAC-888 Pin Description

SYMBOL	DESCRIPTION	
DB_0 - DB_7	DATA BIT — Bits 0-7 are digital, active-high inputs. DB_7 is assigned as the MSB.	PINS 1-8
$\overline{CE}$	CHIP ENABLE — An active low input control which is the device enable input terminal.	PIN 17
$\overline{WR}$	WRITE CONTROL — An active low control which enables the microprocessor to write data to the DAC.	PIN 16
I_{OUT} • $\overline{I_{OUT}}$	CURRENT OUTPUT — Complementary current outputs, which when added, equal I_{FS}.	PINS 13-14
V_{REF+}, V_{REF-}	VOLTAGE REFERENCE — Differential inputs that accept a negative, positive, or bipolar input and are used to set I_{FS}.	PINS 10-11
COMP	COMPENSATION — The reference amplifier frequency compensating terminal.	PIN 12

Functional Diagram and Timing Diagram for 8-Bit Operation





NOTE: IF INPUT DATA CHANGES AFTER ($\overline{WR} \bullet \overline{CE}$) LOW AND BEFORE ($\overline{WR} \bullet \overline{CE}$) HIGH - t_{DS}|, $I_{OUT}/\overline{I_{OUT}}$ WILL CHANGE. THE LAST DATA BEFORE ($\overline{WR} \bullet \overline{CE}$) HIGH - t_{DS}| WILL BE LATCHED PROVIDED DATA VALID IS HELD FOR ($t_{DS\ (MIN)}$ - $t_{DH\ (MIN)}$).

Operating Table

$\overline{CE}$	$\overline{WR}$	OUTPUT
I	X	NO CHANGE
O	I	NO CHANGE
O	O	UPDATE LATCHES (TRANSPARENT)