



# MU9C3480 LANCAM<sup>®</sup>

## ADVANCE INFORMATION

### DISTINCTIVE CHARACTERISTICS

- 256 entries of 64 bits each for storage of addresses plus associated data in a Content-addressable Memory for Fully-associative table look-up
- Configurable on 16-bit boundaries into CAM vs. RAM for application flexibility
- Two Validity bits allow each entry to be separately designated as Valid, Empty, Skipped, or RAM-only
- Dual masks permit further qualification of compare or write operations
- Simple four-wire control for ease of implementation along with an extensive instruction set for flexibility
- Separate Match Flag and Full Flag daisy-chain systems allow devices to be cascaded to any depth
- Perfect for small Workgroup bridges or other LAN applications
- 32-pin PLDCC package for minimum space utilization and 44-pin PLDCC package for compatibility with the MU9C1480
- CMOS technology with a single +5V supply

### GENERAL DESCRIPTION

The MU9C3480 is a 256 entry version of the MU9C1480 LANCAM for applications, such as Workgroup bridges, that require a smaller station list to accomplish positive and/or negative filtering. Each entry in the MU9C3480 is organized as 64 bits of CAM that are configurable on 16-bit boundaries as CAM or RAM to allow for a variety of comparand widths along with Associated data fields for translation storage, port ID storage, time-stamping, or pointers to external virtual memory

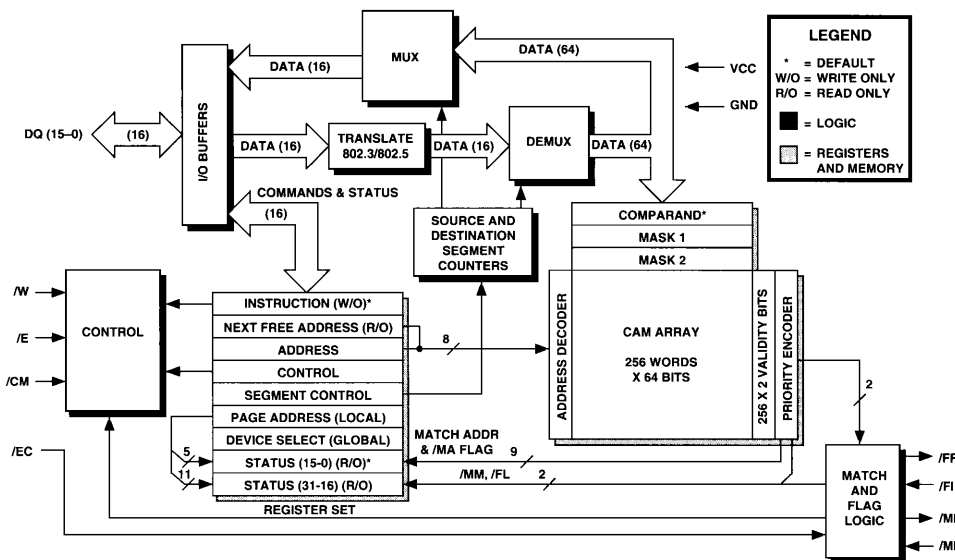
As a member of the LANCAM family, control is performed over a four-wire bus that selects the type of operation to be performed coupled with a 16-bit bi-directional data bus, over which instructions and data are communicated to the device. In normal operation, the Comparand register is loaded with the search tag, and the entire contents of the CAM Memory are automatically compared with the data in the Comparand register. If a match is found, the /MF flag is asserted, the Status register is loaded with the location in CAM Memory of the matching entry, which can itself be used as a pointer or offset to

external memory, and the associated data can be directly read from memory. If there is a no-match, the data can be quickly learned by moving it to the first empty memory location through a Move instruction.

Entries in memory are tagged with two Validity bits that allow each location to be considered Valid and to be included in all compare operations, or Empty, Skipped, or RAM-only, in which case they are not included in compare operations. Separate Segment counters control the writing and reading processes for maximum flexibility. Registers can be directly loaded and read for ease in initialization and housekeeping activities.

The MU9C3480 includes dual mask registers for modifying the conditions of a compare or a write operation, the ability to write immediately after a no-match condition, and the ability to read the Validity bits of the last read memory location.

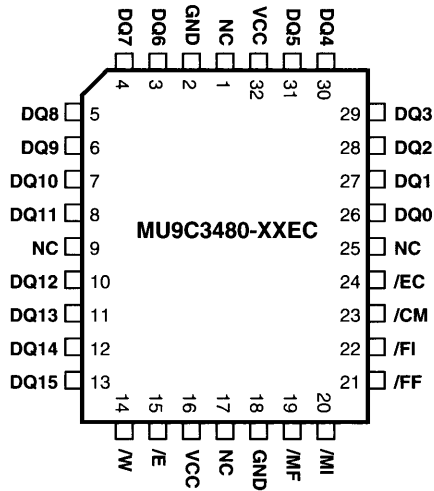
### BLOCK DIAGRAM



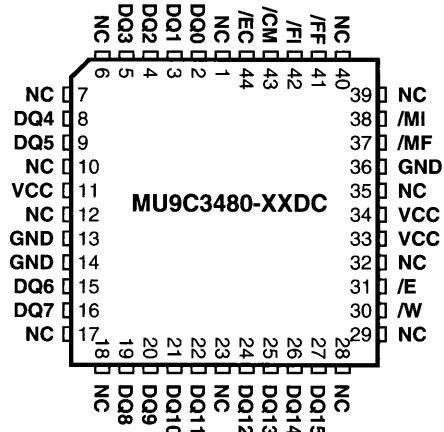
MUSIC016\*

# MU9C3480

## PINOUT DIAGRAMS



32-Pin PLDCC



44-Pin PLDCC

## ORDERING INFORMATION

PART NUMBER	COMPARE CYCLE TIME	TEMPERATURE RANGE
MU9C3480-90EC, -90DC	90 ns	0-70°
MU9C3480-12EC, -12DC	120 ns	0-70°

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