FAIRCHILD SEMICONDUCTOR™

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DM74LS181
4-Bit Arithmetic Logic Unit

General Description

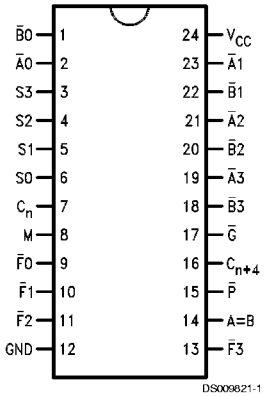
The 'LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

Features

- Provides 16 arithmetic operations: add, subtract, compare, double, plus twelve other arithmetic operations
- Provides all 16 logic operations of two variables: exclusive-OR, compare, AND, NAND, OR, NOR, plus ten other logic operations
- Full lookahead for high speed arithmetic operation on long words

Connection Diagram

Dual-In-Line Package



DS009821-1

Order Number DM54LS181J, DM54LS181W or DM74LS181N
See Package Number J24A, N24A or W24C

Pin Names	Description
$\overline{A}0$–$\overline{A}3$	Operand Inputs (Active LOW)
$\overline{B}0$–$\overline{B}3$	Operand Inputs (Active LOW)
S0–S3	Function Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F}0$–$\overline{F}3$	Function Outputs (Active LOW)
A = B	Comparator Output
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
C_{n+4}	Carry Output

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS181		DM74LS181			Units
		Min	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2		2			V
V_{IL}	Low Level Input Voltage		0.7			0.8	V
I_{OH}	High Level Output Current		−0.4			−0.4	mA
I_{OL}	Low Level Output Current		4			8	mA
T_A	Free Air Operating Temperature	−55	125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	M input			0.1	mA
		V_I = 10V (DM54)	$\overline{A}_n$, $\overline{B}_n$			0.3	
			S_n			0.4	
			C_n			0.5	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	M input			20	µA
			$\overline{A}_n$, $\overline{B}_n$			60	
			S_n			80	
			C_n			100	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	M input			−0.4	mA
			$\overline{A}_n$, $\overline{B}_n$			−1.2	
			S_n			−1.6	
			C_n			−2.0	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, $\overline{B}_n$, C_n = GND	DM54			35	mA
		S_n, M, $\overline{A}_n$ = 4.5V	DM74			37	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics:

for test waveforms and output load. V_{CC} = 5V, T_A = 25˚C

Symbol	Parameter	Conditions	DM54/DM74LS C_L = 15 pF		Units
			Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}	M = GND		27 20	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{F}$	M = GND		26 20	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$ (Sum)	M, S_1, S_2 = GND; S_1, S_3 = 4.5V		29 23	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$ (Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		32 26	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$ (Sum)	M, S_1, S_2 = GND; S_0, S_3 = 4.5V		30 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$ (Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		30 33	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$(Sum)	M, S_1, S_2 = GND; S_0, S_3 = 4.5V		32 25	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$(Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		32 33	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$ (Logic)	M = 4.5V		33 29	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4} (Sum)	M, S_1, S_2 = GND; S_0, S_3 = 4.5V		38 38	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4} (Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		41 41	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to A = B	M, S_0, S_3 = GND; S_1, S_2 = 4.5V; R_L = 2 kΩ to 5.0V		50 62	ns

Sum Mode Test Table 1 Function Inputs

S0 = S3 = 4.5V, S1 = S2 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}

Sum Mode Test Table 1 Function Inputs (Continued)

S0 = S3 = 4.5V, S1 = S2 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

Diff Mode Test Table 2 Function Inputs

S1 = S2 = 4.5V, S0 = S3 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

Logic Mode Test Table 3 Function Inputs

S1 = S2 = M = 4.5V, S0 = S3 = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$

Functional Description

The 'LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the ADD mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the SUBTRACT mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four 'LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Function Table

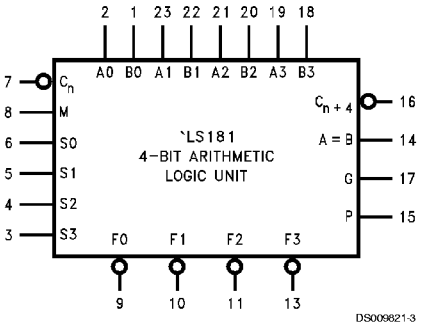
Mode Select Inputs				Active LOW Operands & F_n Outputs		Active HIGH Operands & F_n Outputs	
				Logic	Arithmetic (Note 5)	Logic	Arithmetic (Note 5)
S3	S2	S1	S0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A + B}$	$A\overline{B}$ minus 1	$\overline{A}$ B	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A + B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A $\oplus$ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}$ B	A plus (A + B)	$\overline{A}$ + B	A plus AB
H	L	L	H	A $\oplus$ B	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A (Note 4)	Logic 1	A plus A (Note 4)
H	H	L	H	$A\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

Note 4: Each bit is shifted to the next most significant position.

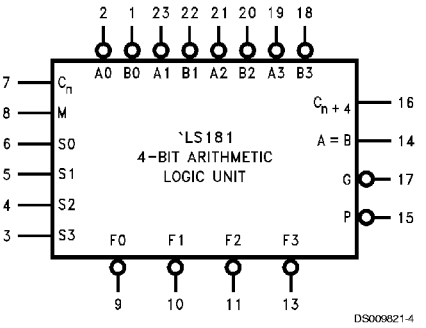
Note 5: Arithmetic operations expressed in 2s complement notation.

Logic Symbols

Active High Operands

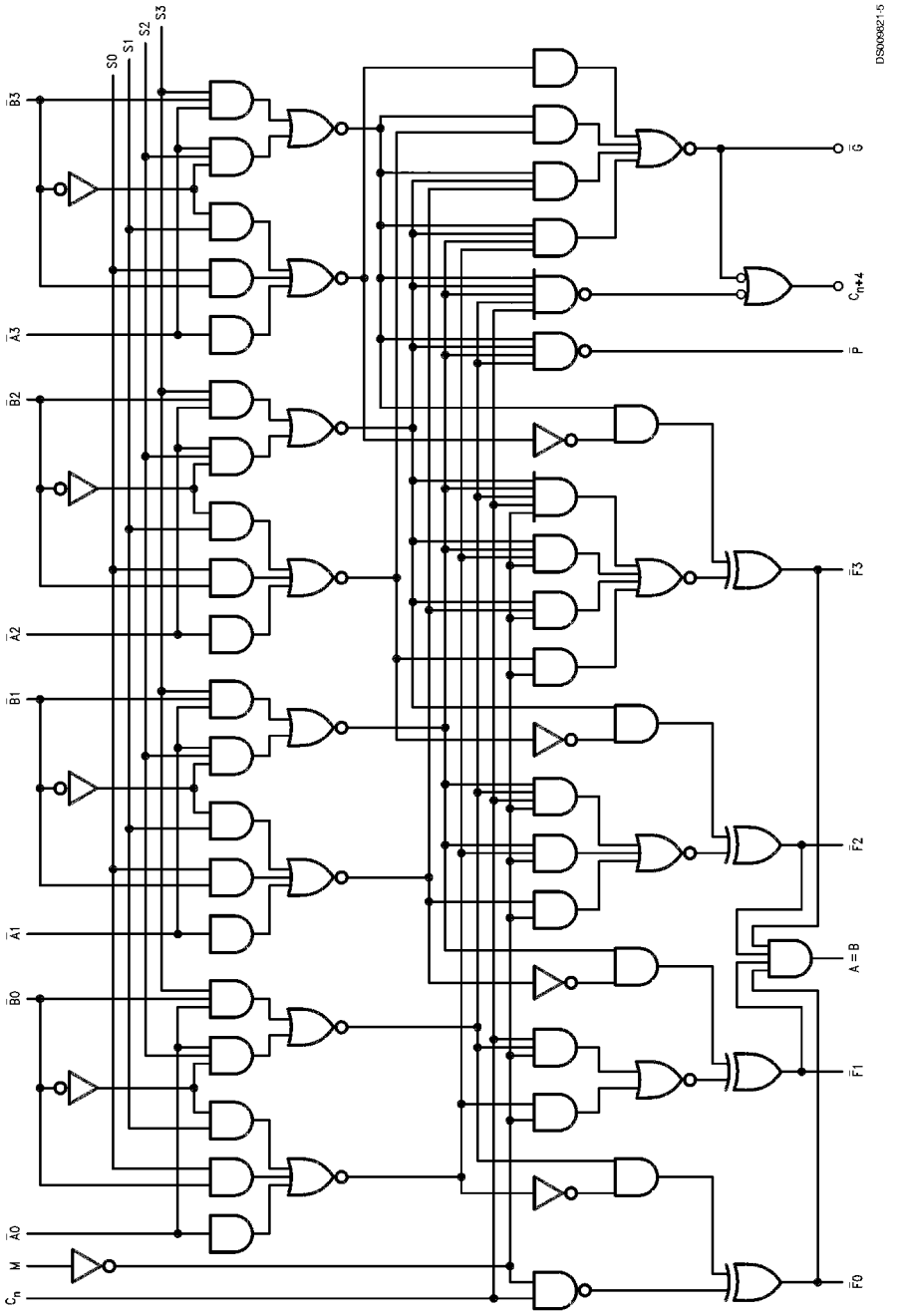


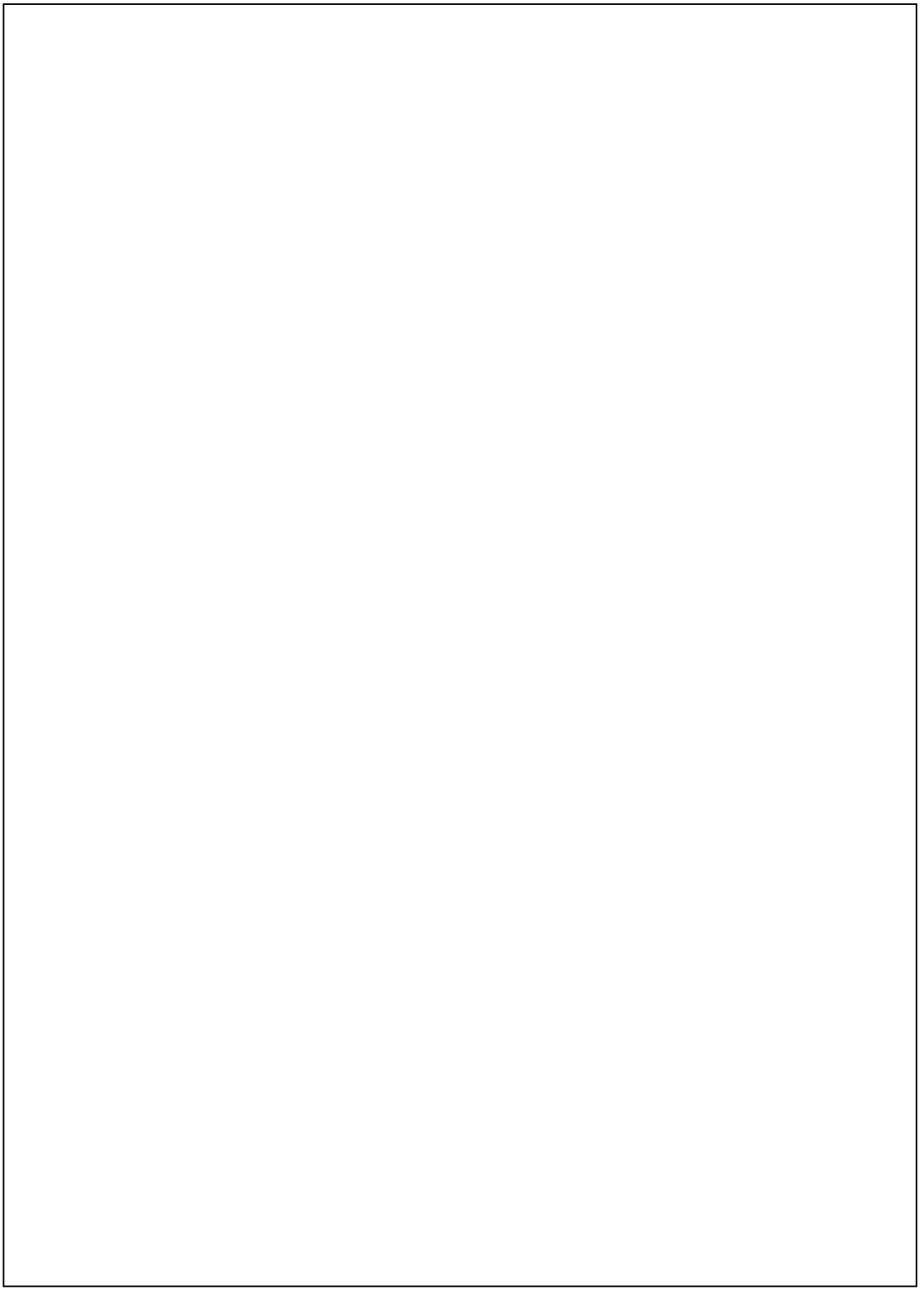
Active Low Operands



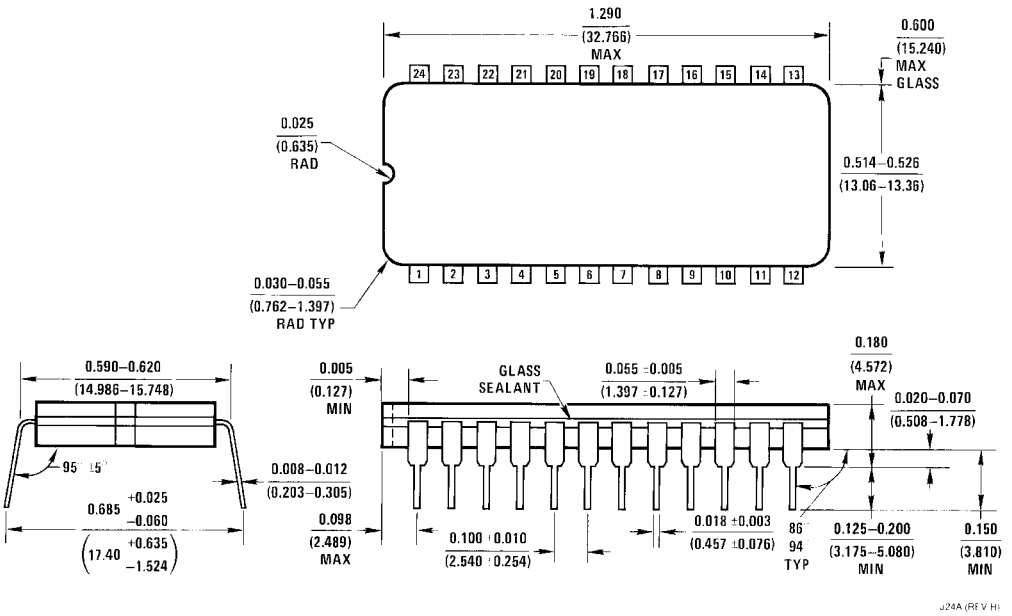
V_{CC} = Pin 24
GND = Pin 12

Logic Diagram

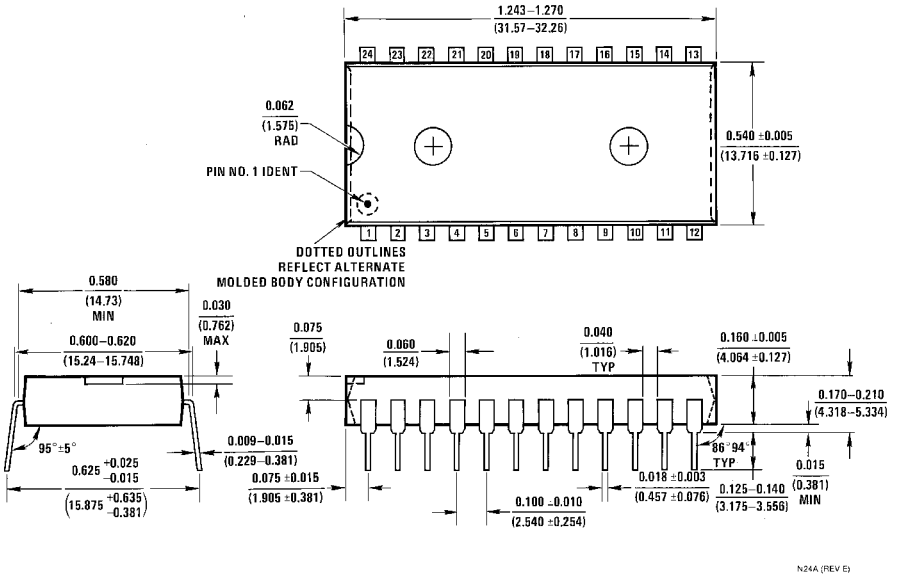




Physical Dimensions inches (millimeters) unless otherwise noted

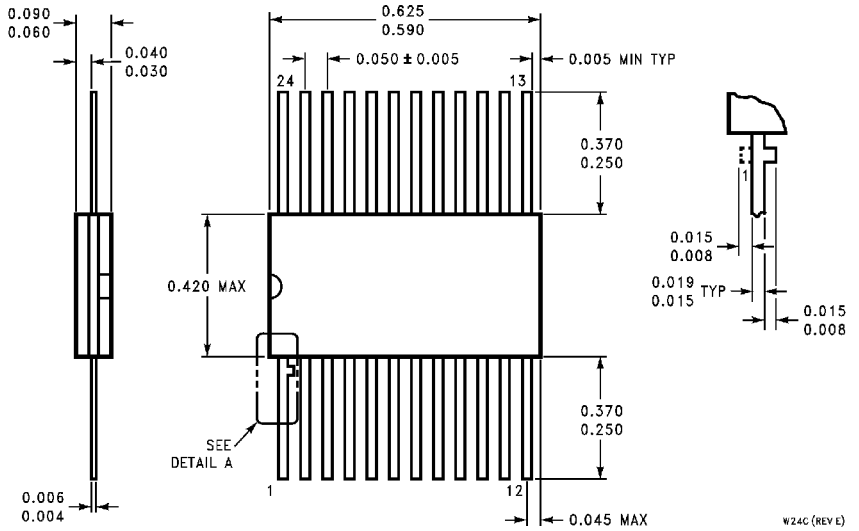


Package (J)
Order Number DM54LS181J
Package Number J24A



24-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS181N
Package Number N24A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Package (W)
Order Number DM54LS181W
Package Number W24C

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