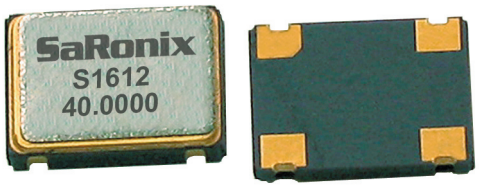
SaRonix™
A PERICOM® COMPANY

S1612 Series

1.8V CMOS Low Jitter Crystal Clock Oscillator (XO)



Actual Size = 5 x 7mm

Product Features

- 1.8V CMOS compatible logic levels
- Pin-compatible with standard 5x7mm packages
- Designed for standard reflow and washing techniques
- Low power standby mode
- Pb-free and RoHS/Green compliant

Product Description

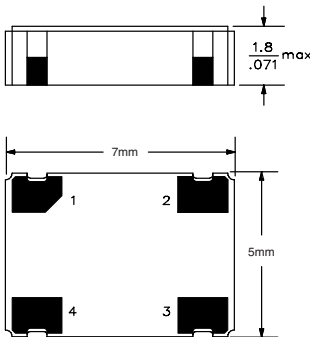
The S1612 Series is a 1.8V crystal clock oscillator using less than 20mW. The output clock signal, generated internally with a non-PLL oscillator design, is compatible with JESD8-7 logic levels. The device, available on tape and reel, is contained in a 5x7mm surface-mount ceramic package.

Applications

The S1612 Series is an ideal reference clock for applications requiring low jitter oand low power, including:

- Portable Electronics
- Server & Storage platforms
- 802.11a/b/g WiFi

Packaging Outline



Pin Functions

Pin	Function
1	OE Function
2	Ground
3	Clock Output
4	V_{DD}

Common Frequencies

Contact SaRonix for additional frequencies

1.5440 Mhz	20.0000 MHz	38.8800 MHz
2.0480 MHz	22.0000 MHz	40.0000 MHz
3.6864 MHz	24.5760 MHz	44.0000 MHz
8.0000 MHz	25.0000 MHz	44.7360 MHz
10.0000 MHz	32.0000 MHz	48.0000 MHz
14.3181 MHz	32.7680 MHz	50.0000 MHz
16.0000 MHz	33.0000 MHz	60.0000 MHz
16.3840 MHz	34.3680 MHz	66.0000 MHz
18.4320 MHz	35.3280 MHz	66.6667 MHz
19.4400 MHz		

Ordering Information

S 1612 B - 25.0000 (T)

- S — SaRonix
- 1612 — Product Series
- B — Frequency Stability: B = ±50 ppM (0 to +70 °C)
- 25.0000 — Output Frequency (MHz)
- (T) — Packaging: (T) = Tape & Reel full reel increments; Blank = Bulk packaged

Electrical Performance

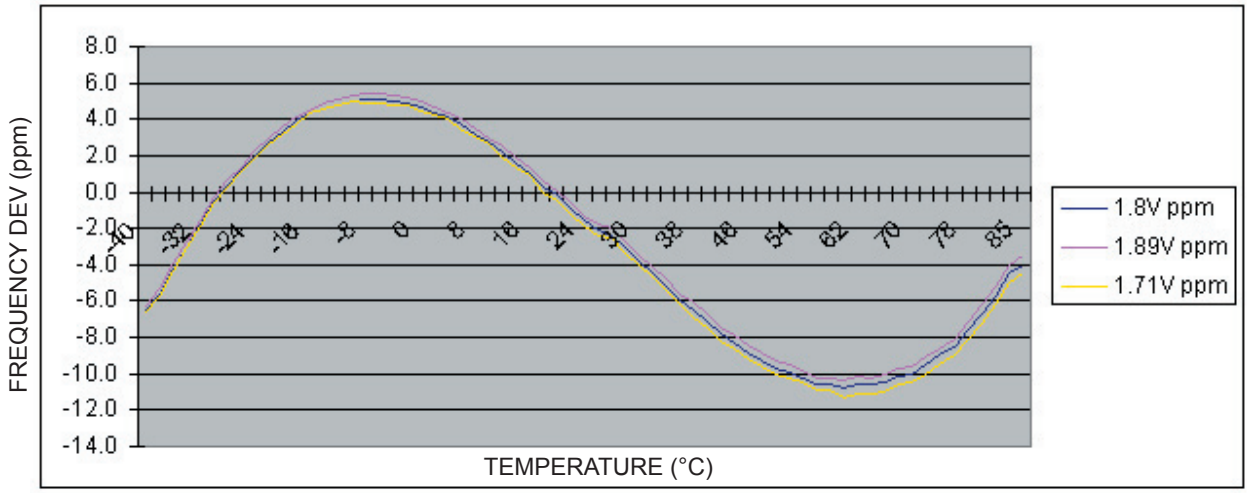
Parameter		Min.	Typ.	Max.	Units	Notes
Output frequency		1.544		70	MHz	As specified
Supply voltage		+1.71	+1.8	+1.89	V	
Supply current, output enabled				4	mA	<36 MHz
				7		36 to 50 MHz
				10		>50 to 70 MHz
Supply current, standby mode				10	µA	1.544 to <36 MHz
				100	µA	36 to 70 MHz
Frequency stability				±50	ppM	See Note 1 below
Operating temperature		0		+70	°C	As specified
Output logic 0, VOL				10% V_{DD}	V	
Output logic 1, VOH		90% V_{DD}			V	
Output load		15 pF (max)				
Duty cycle		45		55	%	measured 50%VDD
Rise and fall time	up to <36 MHz			4	ns	measured 20/80% of waveform
	36 to 70 MHz			2.5		

Notes:
1. As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (1 year at 25°C average effective ambient temperature), shock and vibration.

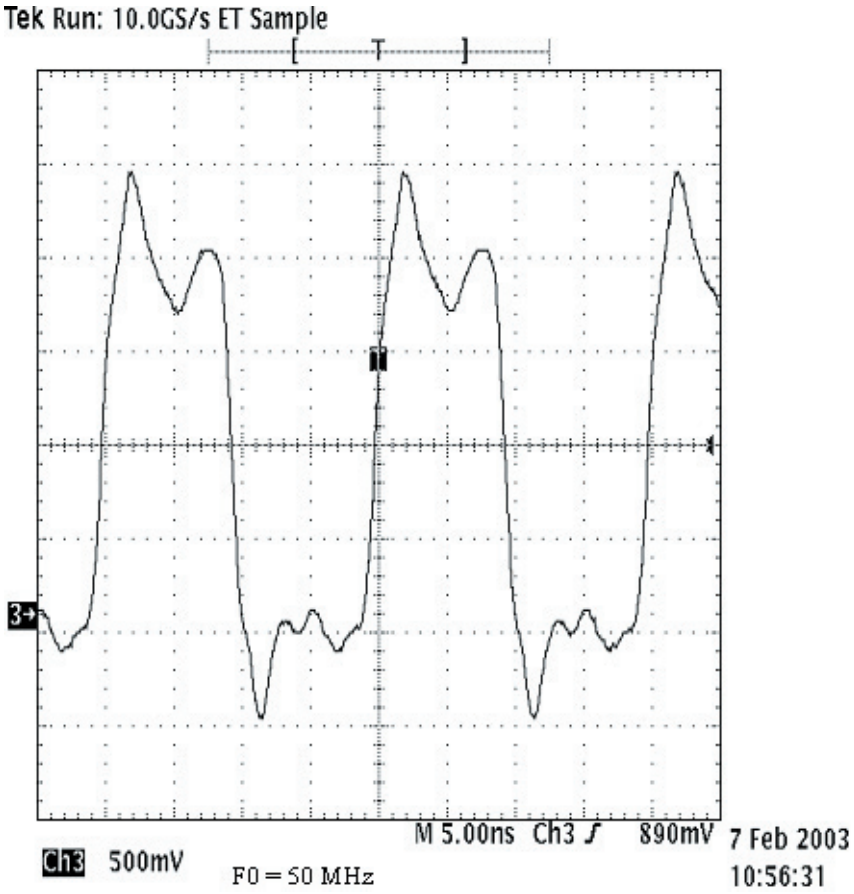
Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	0.7V_{DD}			V	or open
Input voltage (pin 1), Output Disable (low power standby)			0.3V_{DD}	V	Output is Hi-Z
Internal pullup resistance	30			kΩ	
Output disable delay			200	ns	
Output enable delay			10	ms	

Typical Frequency Stability



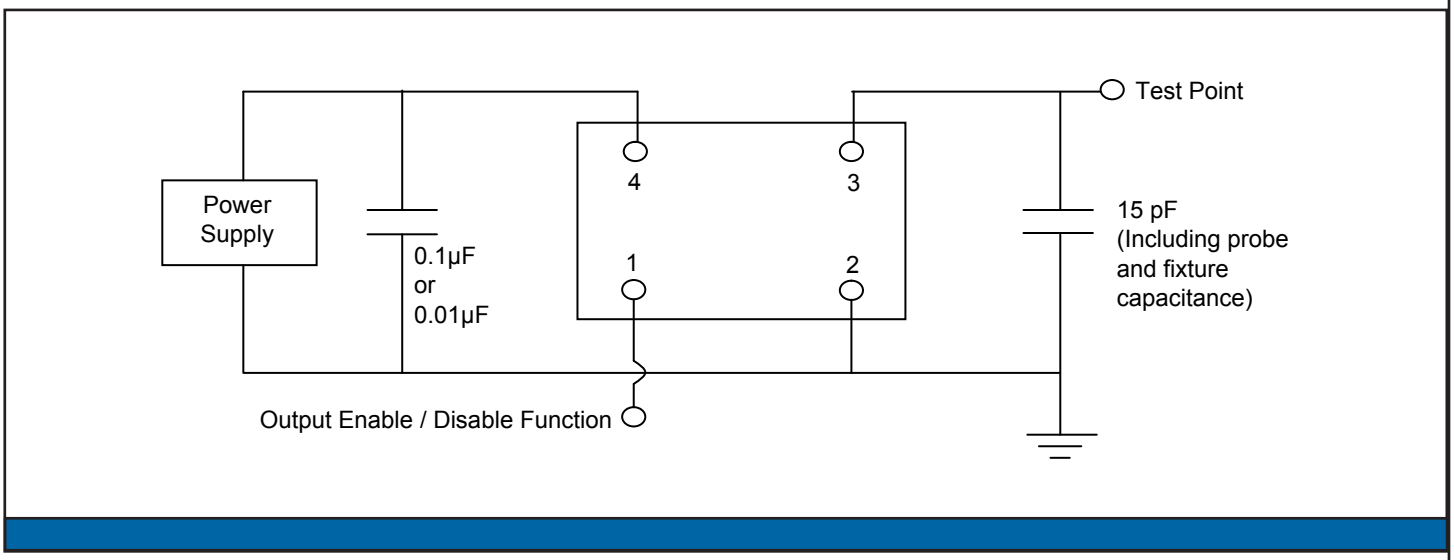
Typical Output Waveform



Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	

Test Circuit

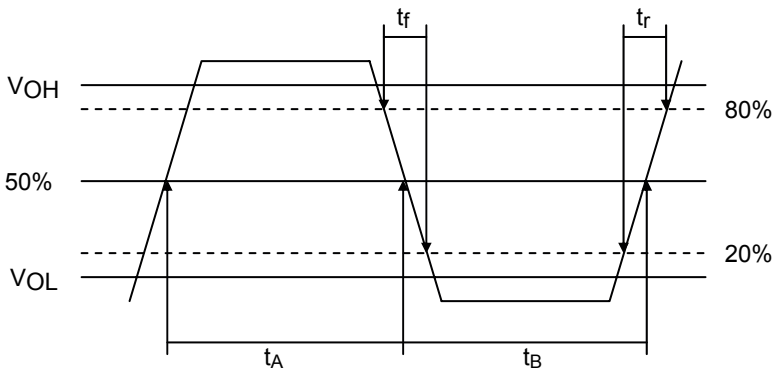


Reliability Test Ratings

This product is rated to meet the following test conditions:

Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2x10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

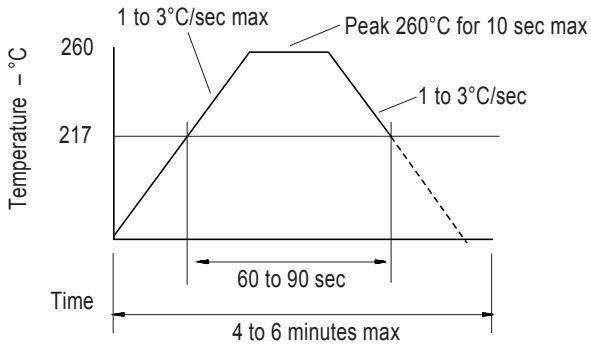
Output Waveform



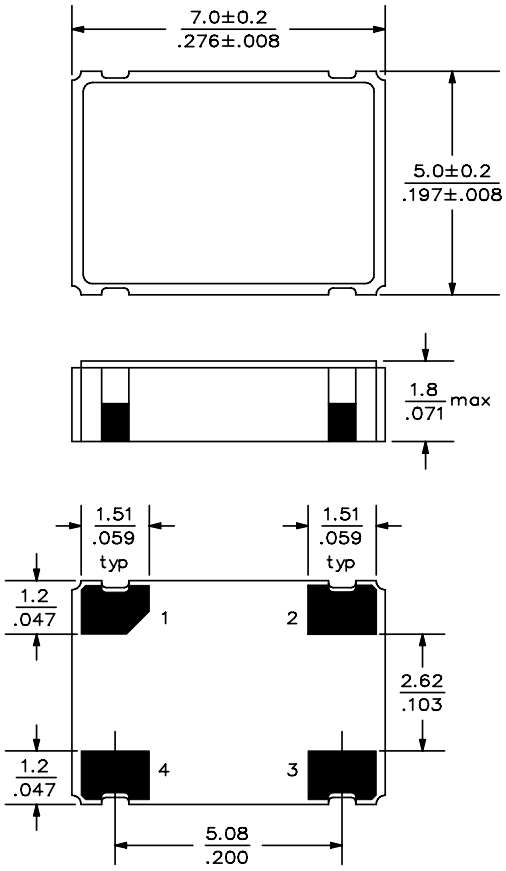
Duty cycle = 100% × (t_A) / (t_A + t_B)

Reflow Soldering Profile

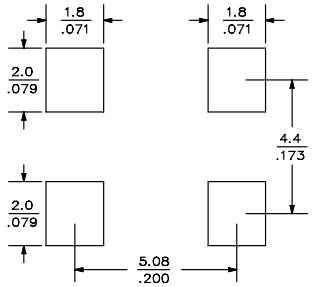
As per IPC/JEDEC J-STD-020C



Mechanical Drawings



Recommended Land Pattern*



*External high-frequency power decoupling is recommended.(see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions are in mm/inches.

Marking LINE 1:	**S M X**	**(SaRonix, Model, Stability code)**
Marking LINE 2:	**Frequency**	**(Frequency code)**
Marking LINE 3:	**● YY WW X**	**(Pin 1, Year, Week, Origin)**

**Exact location of markings may vary.