VOICE OTP IC

*a*P23682 – 682sec

*a*P23341 – 341sec

*a*P23170 – 170sec

*a*P23085 – 85sec

8 PIN

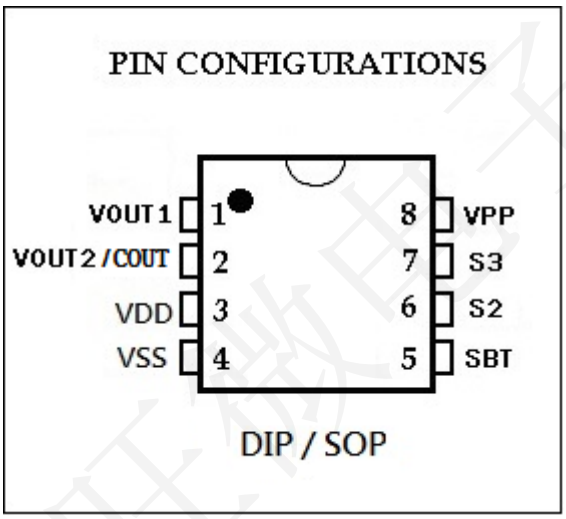
▪ FEATURES :

- Standard CMOS process.
- Embedded 16M/8M/4M/2M EPROM.
- **682/341/170/85** sec Voice Length at 6KHz sampling and 4-bits ADPCM compression.
- Maximum 1024 voice groups.
- Maximum 48KHz sample rate.
- Combination of voice blocks to extend playback duration.
- User selectable PCM16 or ULAW8 or PCM8 or ADPCM4 data compression.
- 5 triggering modes are available :
  - Key Mode :
    S2 ~ S3 to trigger up to 3 voice groups; Power on play function.
  - SBT Mode :
    SBT to trigger up to 1024 voice groups sequentially; Power on play function.
  - SPI Mode : CSB , SCK , DI.
    3 wire address control up to 1024 voice groups.
  - I2C Mode : SCK , DI.
    2 wire address control up to 1024 voice groups.
  - MP3 Mode :
    S2: Forward , S3:Stop.
    SBT: (Play/Pause) or (Play/Sop) Trigger up to 1024 voice groups.
- Voice Group Trigger Options: Edge / Level; Hold / Unholdable; Retrigger / Non-retrigger.
- Optional 16ms or 65us selectable debounce time.
- RST pin set HIGH to stop the playback at once.
- LVD (Low voltage detect).
- Programmable outputs pin out1:
  (*Note: When Key Mode or I2C Mode the SBT pin as output1 use.)
  for busy-H , busy-L , stop-H , stop-L , prog busy-H , prog busy-L , Loadbit,
  LED flash (LED high active) , ~LED flash (LED low active).
- One kind oscillator: Internal-Rosc.
- 2V – 5V single power supply and < 5uA low stand-by current.
- 16/8/4 level volume control setting available.
- 16 bits audio out.
- PWM Vout1 and Vout2 drive speaker directly.
- D/A COUT pin drives speaker through an external BJT or audio AMP.
- Development System support for voice compilation.

▪ DESCRIPTION :

aP23682/341/170/085 series high performance Voice OTP is fabricated with Standard CMOS process with embedded 16M/8M/4M/2M bits EPROM. It can store up to 682/341/170/85 sec voice message with 4-bits ADPCM compression at 6KHz sampling rate. 16-bits PCM、8-bits PCM and 8-bits ULAW at (4K to 48K sample rate) is also available for user selecting.

User selectable triggering and output signal options provide maximum flexibility to various applications. Built-in resistor controlled oscillator, 16-bits current mode DAC output and 14-bits PWM direct speaker driving output minimize the number of external components. PC controlled programmer and developing software are available.



▪ PIN NAMES :

PIN (8-pin)	Playback Mode	OTP Program Mode	Description
1	VOUT1		PWM output to drive speaker directly.
2	VOUT2/COUT		PWM output to drive speaker directly. / DAC current output.
3	VDD	VDD	Supply voltage.
4	VSS	VSS	Supply ground.
5	SBT	SBT	Trigger pin (I/O pin with internal pull-down).
6	S2	S2	Trigger pin (I/O pin with internal pull-down).
7	S3	S3	Trigger pin (I/O pin with internal pull-down).
8	VPP	VPP	Supply ground.

▪ PIN DESCRIPTIONS :

S2 ~ S3

Input Trigger Pins:
- In Key Mode :S2 and S3 is used to trigger 3 Voice groups.
- In SPI Mode :
  S2 is the Serial Clock (SCK) pin which clocks the input command and data bits into the chip.
  S3 is the Data In (DI) pin in which command and data bits are shifted input into the chip.
- In I2C Mode :
  S2 is the Serial Clock (SCK) pin which clocks the input command and data bits into the chip.
  S3 is the Data In (DI) pin in which command and data bits are shifted input into the chip.
- In MP3 Mode :
  S2 :Forward. S3:Stop.

SBT

Input Trigger Pin:
- In SBT Mode : This pin is trigger pin to play Voice Groups one time or looping sequentially up to 1024 Voice Groups.
- In SPI Mode : SBT is Chip Select (CSB) pin to initiate the command input.
- In I2C Mode : SBT as output1 use.
- In MP3 Mode: SBT pin is (Play/Pause) or (Play/Sop).

VDD

Power Supply Pins : This pins must be connected to the positive power supply.

VPP

During voice playback, this pin and VSS must be connected together to the power ground.
In Circuit Program : This pin is connected to a separate 8.5V power supply voltage for OTP programming. Connect resistor between power ground and VPP.
Note : Resistor is 10K Ω.

VSS

Power Ground Pins : VSS and VPP pins must be connected together to the power ground during voice playback.
In Circuit Program : VSS and VPP pins must be separated to the power ground. Connect resistor between power ground and VPP.

VOUT1 and VOUT2

14-bits PWM output pins which can drive speaker and buzzer directly for voice playback.

COUT

16-bits current mode DAC output for voice playback.

OUT1 (When SBT pin as OUT1 use)

OUT1 can select output function as below :
1. Busy- H : When voice is playing, output high level signal.
2. Busy- L : Inverted output of Busy- H.
3. LED- Flash : When voice is playing, output LED flash pulse.
4. ~LED- Flash : Inverted output of LED- Flash.

5. Stop- H : When voice plays finished, output stop pulse.
6. Stop- L : Inverted output of Stop- H.
7. LoadBit : After load voice data to buffer success, output logic high signal.
8. Prog-Busy - H : When voice of Prog-Busy set 1, high pulse output.
   When voice of Prog-Busy set 0, low pulse output.
9. Prog-Busy - L : Inverted output of Prog-Busy - H.

▪ VOICE SECTION COMBINATIONS :

Voice files created by the PC base developing system are stored in the built-in EPROM of the aP23682/341/170/085 chip as a number of fixed length Voice Blocks. Voice Blocks are then selected and grouped into Voice Groups for playback. Up to 1024 Voice Groups are allowed. A Voice Blocks Table is used to store the information of combinations of Voice Blocks and then group them together to form Voice Group.

Chip	**aP23682**	**aP23341**	**aP23170**	**aP23085**
Memory size	16M bits	8M bits	4M bits	2M bits
Max no. of Voice Block	2016	2016	2016	2016
Max. no. of Voice Group	1024	1024	1024	1024
Voice Length (@ 6KHz 4-bit ADPCM)	682 sec	341 sec	170 sec	85 sec

▪ Example of Voice Block Combination :

Assume here we have three voice files, they are “How are You?”, Sound Effect and Music. Each of the voice file is divided into a number of fixed length Voice Block and stored into the memory.
Voice block :

B1 = “How”	B2 = ”are”	B3 = ”You”
B4 = Sound Effect	B5 = Music1	B6 = Music2

Voice Blocks are grouped together using Voice Table to form Voice Group for playback:

Group no.	**Voice Group contents**	**Voice Table Entries**
Group 1	“How are You?”	B1+B2+B3
Group 2	Sound Effect + “How are You?”	B4+ B1+B2+B3
Group 3	“How are You?” + Music1	B1+B2+B3+B5
Group 4	Music2	B6

▪ Voice Data Compression :

Voice File data is stored in the on-chip EPROM as either 4-bits ADPCM or 8-bits PCM/ ULAW format or 16-bits PCM format. Voice data are stored as 16-bits PCM forma is without compression. The voice playback quality is best. Voice data stored as 4-bits ADPCM or 8-bits PCM/ ULAW provide 4:2 data compression to save memory space. But voice playback quality with be lower than 16-bits PCM format.

▪ Group Options :

User selectable options that affect each individual group are called Group Options. They are:

- Edge or Level trigger.
- Unholdable or Holdable option.
- Re-triggerable or Non-retriggerable option.
- Stop pulse disable or enable.

Fig. 1 to Fig. 6 show the voice playback with different combination of triggering mode and the relationship between outputs and voice playback.

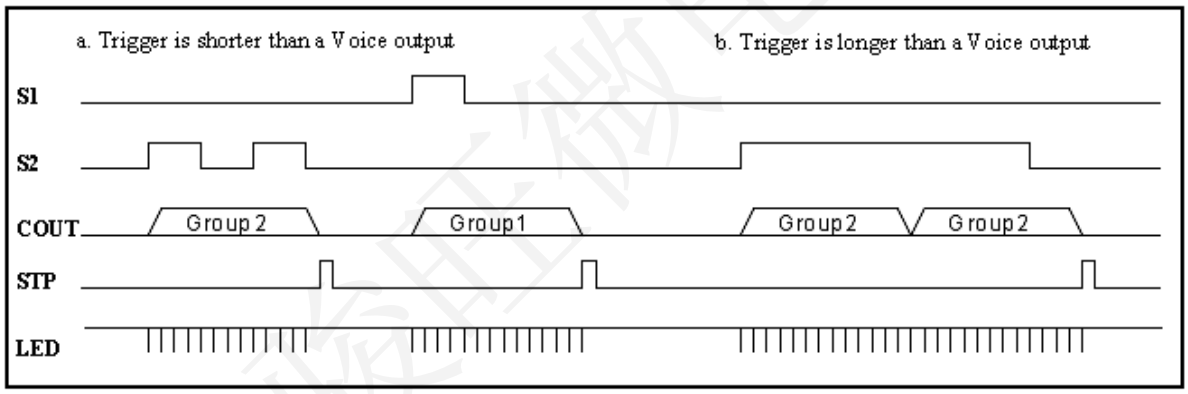


Fig. 1 Level, Unholdable, Non-retriggerable

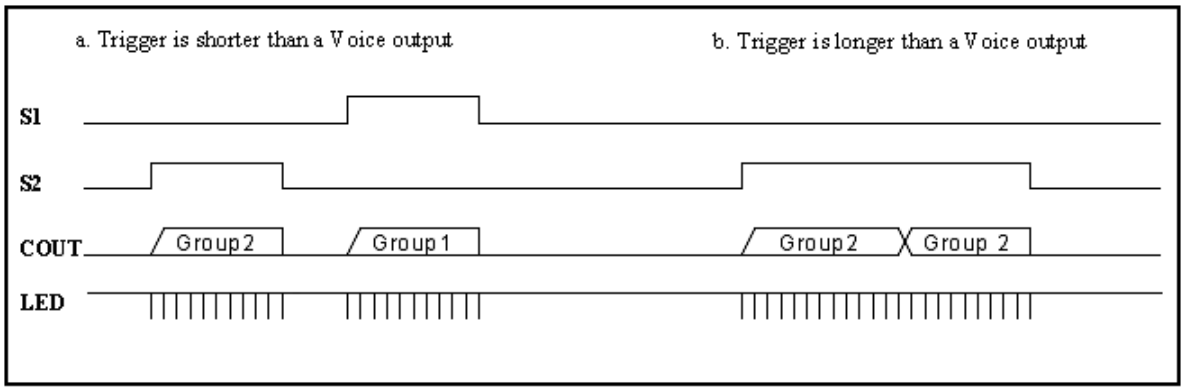


Fig. 2 Level Holdable

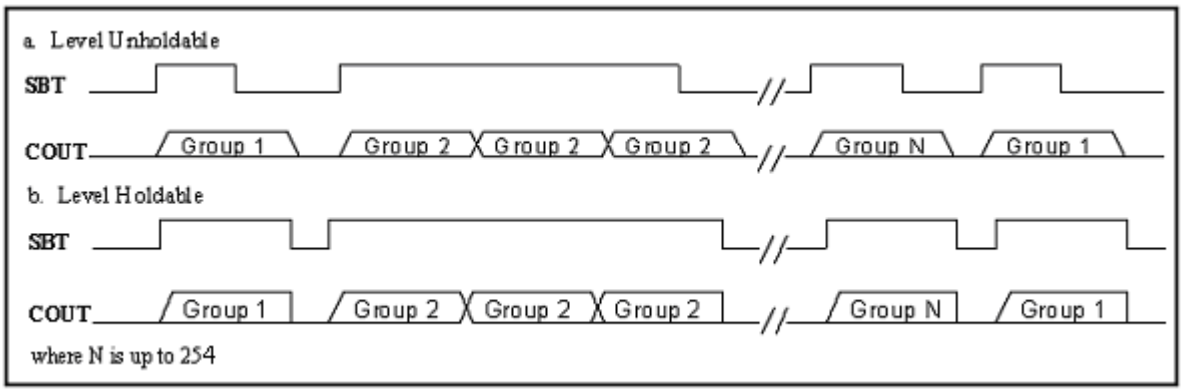


Fig. 3 SBT sequential trigger with Level Holdable and Unholdable

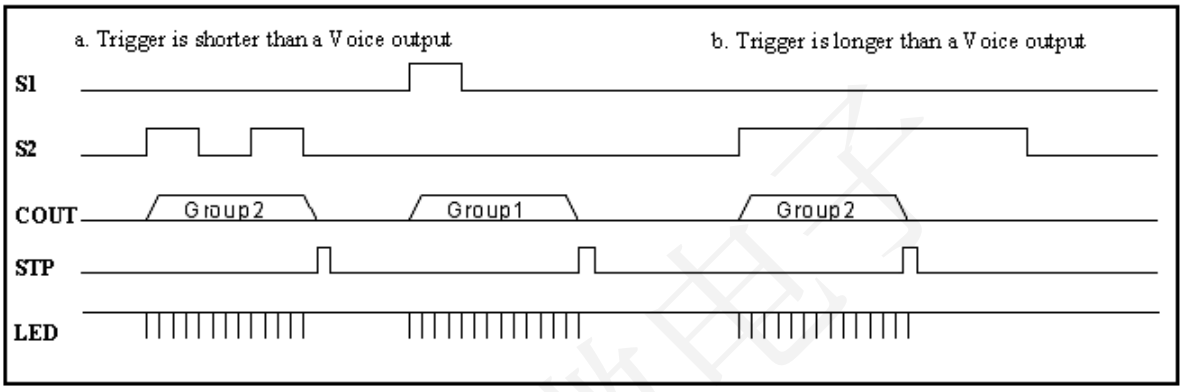


Fig. 4 Edge, Unholdable, Non-retrigger

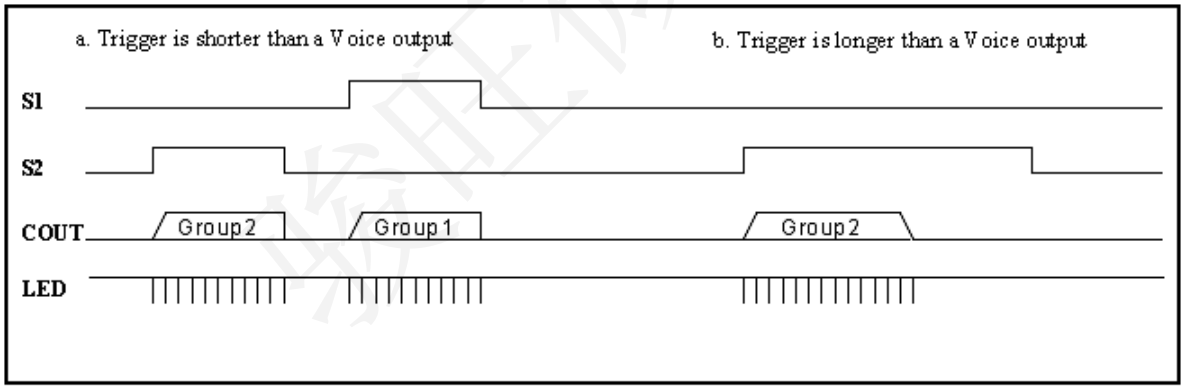


Fig. 5 Edge, Holdable

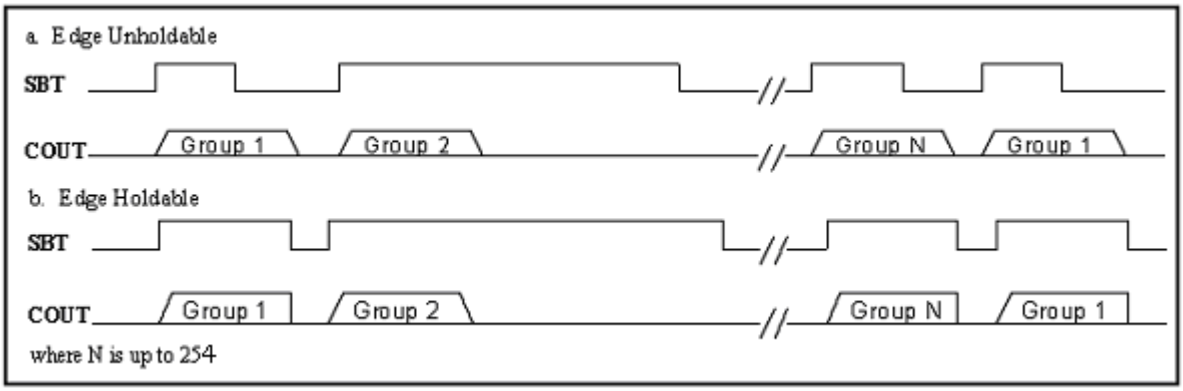


Fig. 6 SBT sequential trigger with Edge Holdable and Unholdable

▪ TRIGGER MODES :

There are five trigger modes available for aP23682/341/170/085 series.

- Key Mode.
- SBT Mode.
- SPI Mode.
- I2C Mode.
- MP3 Mode.

• Key Mode :

With this trigger mode, the beginning 3 Voice Groups are triggered by setting S2 to S3 to HIGH or LOW in different combinations. Each Voice Group can have its only independent trigger options (See Fig. 1,2,4 and 5 for trigger options definition).

· SBT key as key3 (Key3) :

Voice Group	SBT	S3	S2
SW1	NC	NC	HIGH
SW2	NC	HIGH	NC
SW3	NC	HIGH	HIGH
SW4	HIGH	NC	NC
SW5	HIGH	NC	HIGH
SW6	HIGH	HIGH	NC
SW7	HIGH	HIGH	HIGH

· SBT key as output (OUT1) :

The SBT pin compile must be set up [SBT as OUT1]
SBT as OUT1 can select : busy-H/L,stop-H/L,LED flash(LED high active),
~LED flash(LED low active),prog busyH/L, LoadBit.

Voice Group	S3	S2		SBT = OUT1
SW1	NC	HIGH		SBT swap SBT as OUT1
SW2	HIGH	NC		
SW3	HIGH	HIGH		

★★★ Note: NC represents open or no connection

• SBT Mode :

A maximum of 1024 Voice Groups are available. And can be triggered one by one sequentially with the SBT key (See Fig. 3 and 6).

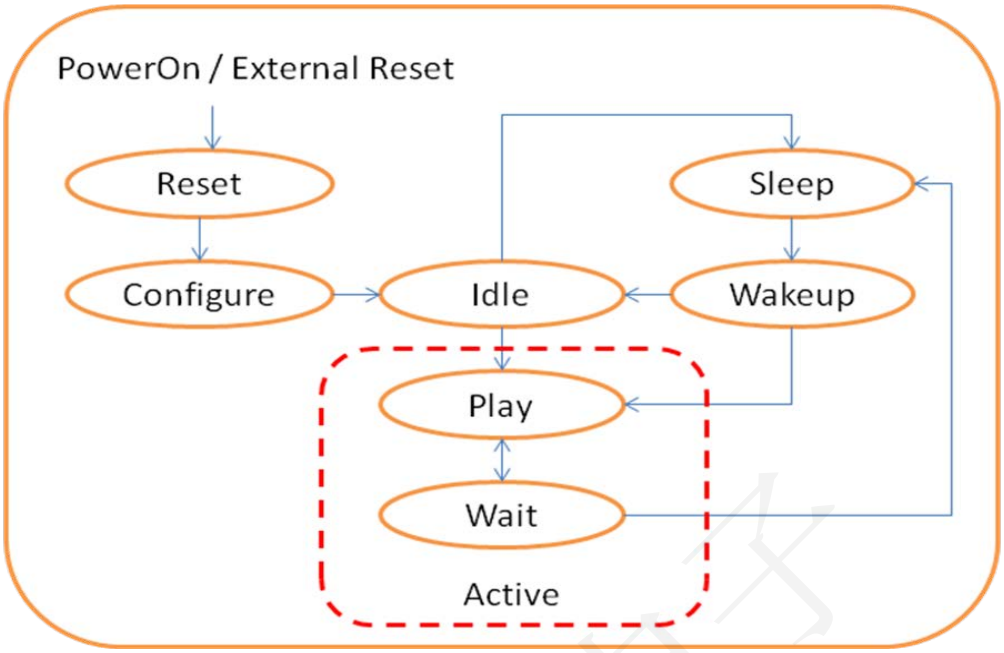
CPU Serial Command Description :

CPU Serial Command include **SPI Mode、I2C Mode.**
The command support to reference Fig.7 CPU Serial Command Description.

LOAD	1. This command pre-load the next Voice Group Address into the address buffer. 2. The "Full/Load" signal will become HIHG once the Group Address is loaded. 3. The Voice Group will be played once the playing of the current Voice Group is finished. 4. The "Full/Load" signal will become LOW once the Voice Group is played and the address buffer is released and ready for next PREFECT action. 5. Using this command make sure there is **no gap** between each Voice Group.
PLAY	1. This command load the Voice Group Address into the address buffer. 2. The current Voice Group will be stopped and play the new one.
PU1	Power up the chip without ramp-up (suitable for PWM direct drive).
PU2	Power up the chip with ramp-up (suitable for COUT transistor drive).
PD1	Power down the chip without ramp-down (suitable for PWM direct drive).
PD2	Power down the chip with ramp-down (suitable for COUT transistor drive).
VOL	Set Volume index of volume Table.
VOL--	Decrease the volume index of volume Table.
VOL++	Increase the volume index of volume Table.
PAUSE	Pause the current Voice Group.
RESUME	Resume the current Voice Group.
REWIND	Play the current Voice Group from it's beginning.

Fig. 7 CPU Serial Command Description

State Description :



State Name	Description
Reset	Include Power On Reset (typ 5us) and external reset (depends on the external reset circuit). All pins are input floating. **Serial Command inhibited**. After reset, state transfer to the " Configure " state.
Configure	Internal Chip Configuration. All pins are input floating. **Serial Command inhibited**. **(Max configure time = 2ms)** After configuration, state transfer to the "Idle" state.
Idle	State transfer to the **"Play"** state if **"active command"** received before timeout. After **time out** without active command, state transition to the **"Sleep"** State.
Play	Playing Voice Group include ramp. State transfer to the "Wait" state if nothing to be played.
Wait	Wait new Serial command and back to the play state without time limit. State transition to the **"Sleep"** state if **"de-active command"** received. Ramp down before transition to the sleep if the "PD2" command be accepted.
Sleep	State transition to the "Wakeup" state if selected by the host CPU. **(Wait sleep to wake up state time = 20us.)**
Wake up	**Single command be buffered and wait to execute after wakeup state!!** **(Max wakeup time = 2ms).** State transition to the "Play" state if active command received else to the "Idle" state.

Fig. 8 State Description

*** Active commands are "Load", "Play", "PU1" and "PU2".
De-Active commands are "PD1" and "PD2".

In CPU Serial Command Control :

a. Using PU1/PU2 command first from de-active state.
Add 2ms delay after PU1/PU2 command is necessary.
b. Max "Output Delay of Busy/Full Signal" equal 2ms during active.
c. Output select to reference PIN DESCRIPTIONS of OUT1

- **SPI Mode :**

This trigger mode is specially designed for simple CPU interface. The aP23682/341/170/085 is controlled by command sent to it from the host CPU. S2 、 S3 and SBT used to input command word into the chip .

- SBT acts as CSB (Chip Select) to initiate the command word input.
- S2 acts as SCK (Serial Clock) to clock-in the command word at rising edge.
- S3 acts as DI (Data-In) to input the command bits.

SPI Command Table [MSB First] : Command input into the chip 16-bits data.

Command	D15	D14	D13	D12	D11	D10	D[9:0]
LOAD	1	0	0	1	0	1	Voice Group Address Number.
PLAY	1	0	0	1	1	0	Voice Group Address Number.
PU1 w/o Ramp	1	0	1	0	0	1	don't care.
PU2 with Ramp	1	0	1	0	1	0	don't care.
PD1 w/o Ramp	1	0	1	1	0	1	don't care.
PD2 with Ramp	1	0	1	1	1	0	don't care.
VOL	0	1	0	0	0	1	0 0 0 0 0 0 VOL[3:0]
VOL--	0	1	0	0	1	0	don't care.
VOL++	0	1	0	1	0	1	don't care.
PAUSE	0	1	1	0	0	1	don't care.
RESUME	0	1	1	0	1	0	don't care.
REWIND	0	1	1	1	0	1	don't care.

Fig. 9 SPI Command Table

SPI Command Timing Diagram:

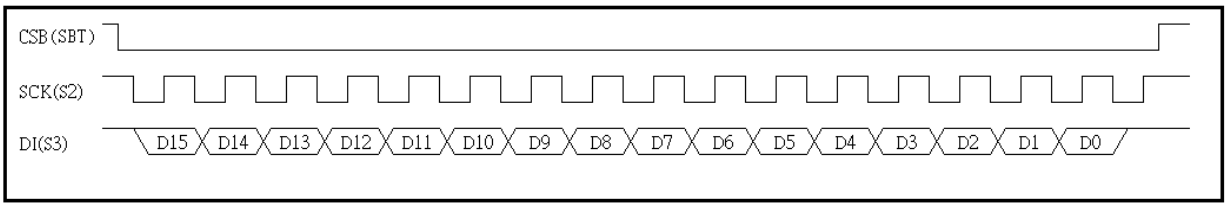


Fig.10 SPI Command timing

* Data is latched at rising edge of SCK.

* SPI Command function reference Fig. 7 CPU Serial Command Description.

Power up with RAMP-UP(PU2) or without RAMP-UP(PU1)

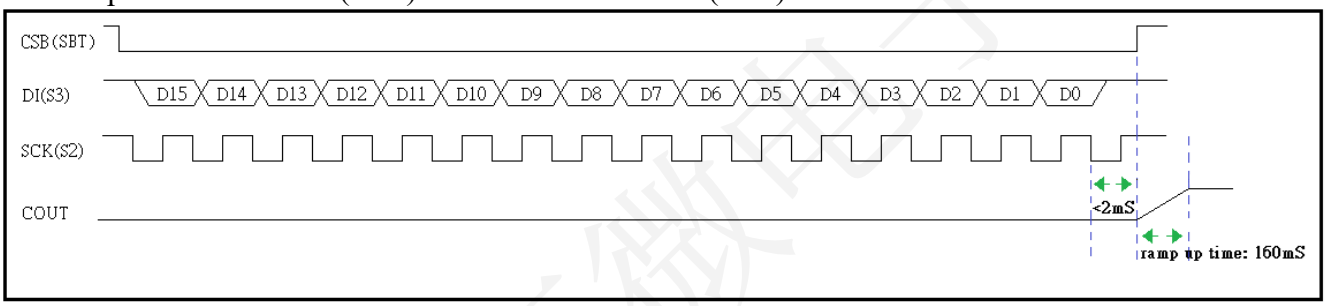


Fig. 11 Power-Up command timing

* Ramp up time : 160mS

Power down with RAMP-DOWN(PD2) or without RAMP-DOWN (PD1)

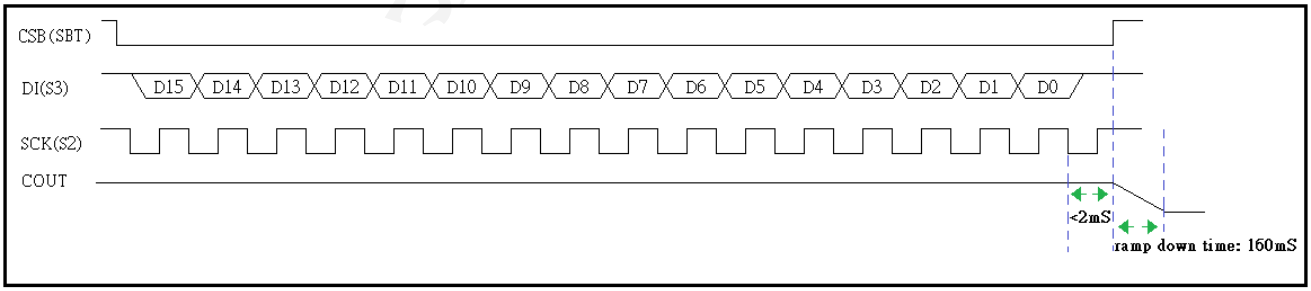


Fig. 12 Power-Down command timing

* Ramp down time : 160mS

(1). Load Voice Group Address :
a. Command timing reference Fig.10 SPI Command timing.
b. D9 to D0 total 10 bits to be the Group Address.
c. The Load signal will become logic LOW once the Voice Group is played and the address buffer is released and ready for next Play action.

(2). Play Voice Group Address :
a. Command timing reference Fig.10 SPI Command timing.
b. D9 to D0 total 10 bits to be the Group Address.
c. Playing assign group address immediately.

(3). Power up with RAMP-UP(PU2) or without RAMP-UP(PU1) :
a. Command timing reference Fig. 11 Power-Up command timing.
b. PU1 : will power-up the chip and set the VOUT to center value immediately and stay there.
c. PU2 : will power-up the chip and ramp-up COUT from bottom to center value and stay there.

(4). Power-down with RAMP-DOWN(PD2) or without RAMP-DOWN (PD1) :
a. Command timing reference Fig. 12 Power-Down command timing.
b. PDN1 will power-down the chip and set the VOUT data to bottom value immediately.
PDN1 will be executed correctly only if PU1 is executed before.
c. PDN2 will power-down the chip and ramp-down the COUT from its current to bottom value.
PDN2 will be executed correctly only if PU2 is executed before.

(5). Volume Set (VOL[3:0]) :
a. Command timing reference Fig.10 SPI Command timing.
b. D3 to D0 total 4bits(0 ~ 15) set volume level (max : 0, min : 15).

(6). Volume - - (VOL--) :
a. Command timing reference Fig.10 SPI Command timing.
b. Set volume level decrease.

(7). Volume + + (VOL++) :
a. Command timing reference Fig.10 SPI Command timing.
b. Set volume level increase.

(8). Pause and Resume (PAUSE; RESUME) :
a. Command timing reference Fig.10 SPI Command timing.
b. In Pause state, VOUT1 and VOUT2 will stay at logic LOW while the COUT will stay at the current D/A data level. When Resume, the COUT data will continue at the current D/A data level.

(9). Rewind :
a. Command timing reference Fig.10 SPI Command timing.
b. Play the current Voice Group from it is beginning.

- **I2C Mode :**

This trigger mode is specially designed for simple CPU interface. The aP23682/341/170/085 is controlled by command sent to it from the host CPU. S2 and S3 are used to input command word into the chip while SBT as OUT1 as output from the chip to the host CPU for feedback response.

- S2 acts as SCK (Serial Clock) to clock-in the command word at rising edge.
- S3 acts as DI (Data-In) to input the command bits.
- SBT acts as BUSY to indicate the chip is in busy state(include play and ramp).

I2C Command Table [MSB First] : Command input into the chip 16-bits data.

Command	D15	D14	D13	D12	D11	D10	D[9:0]
LOAD	1	0	0	1	0	1	Voice Group Address Number.
PLAY	1	0	0	1	1	0	Voice Group Address Number.
PU1 w/o Ramp	1	0	1	0	0	1	don't care.
PU2 with Ramp	1	0	1	0	1	0	don't care.
PD1 w/o Ramp	1	0	1	1	0	1	don't care.
PD2 with Ramp	1	0	1	1	1	0	don't care.
VOL	0	1	0	0	0	1	0 0 0 0 0 0 VOL[3:0]
VOL--	0	1	0	0	1	0	don't care.
VOL++	0	1	0	1	0	1	don't care.
PAUSE	0	1	1	0	0	1	don't care.
RESUME	0	1	1	0	1	0	don't care.
REWIND	0	1	1	1	0	1	don't care.

Fig. 13 I2C Command Table

I2C Command Timing Diagram:

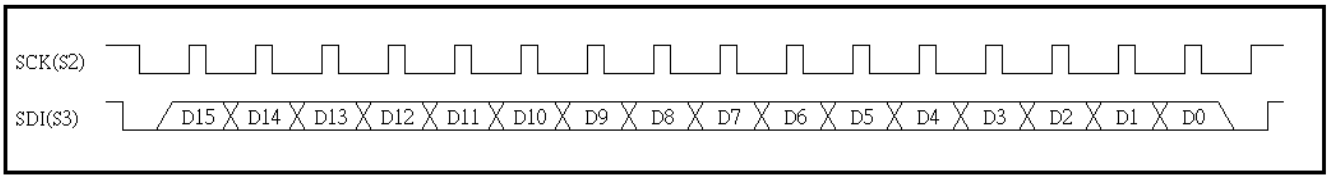


Fig.14 I2C Command timing

* The data bit only can be changed in SCK low level , but it has to be latched before rising edge of SCK.

* I2C Command function reference Fig. 7 CPU Serial Command Description.

Power up with RAMP-UP(PU2) or without RAMP-UP(PU1)

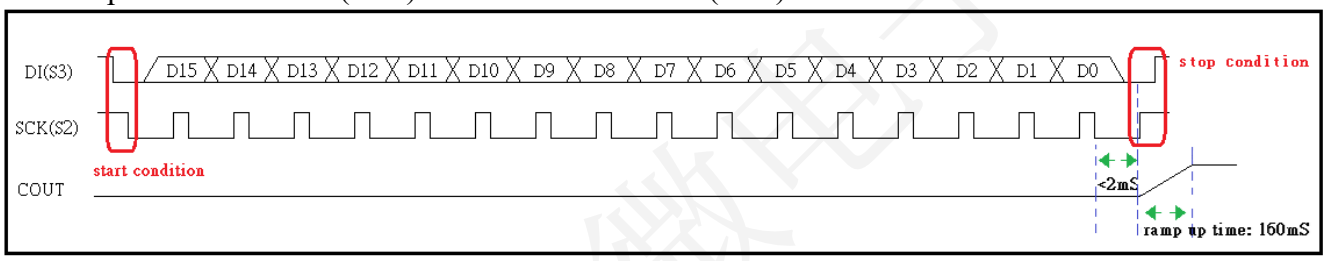


Fig. 15 Power-Up command timing

* Ramp up time : 160mS

Add stop condition after power on and internal chip configuration time finish.
In Power up command : After start condition signal, add delay time more than 300us to wake up device.

Power-down with RAMP-DOWN(PD2) or without RAMP-DOWN (PD1)

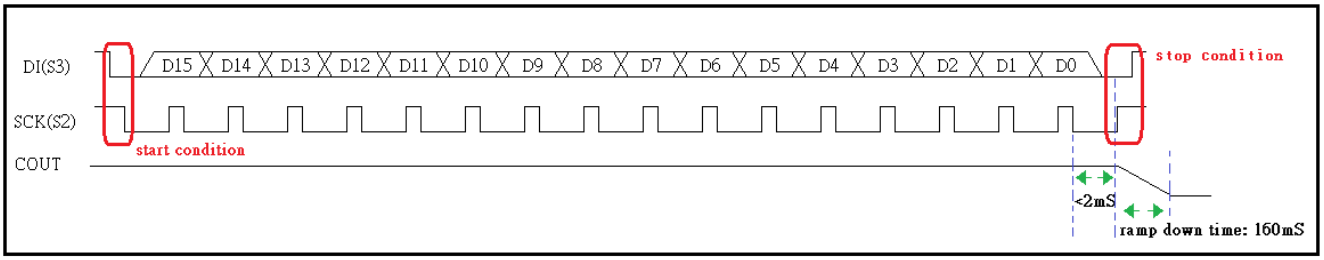


Fig. 16 Power-Down command timing

* Ramp down time : 160mS

(1). Load Voice Group Address :
a. Command timing reference Fig.14 I2C Command timing.
b. D9 to D0 total 10 bits to be the Group Address.
c. The OUT1 output (LoadBit) will become logic high once the Group Address is successfully loaded.
d. The Load signal will become logic LOW once the Voice Group is played and the address buffer is released and ready for next Play action.

(2). Play Voice Group Address :
a. Command timing reference Fig.14 I2C Command timing.
b. D9 to D0 total 10 bits to be the Group Address.
c. Playing assign group address immediately.

(3). Power up with RAMP-UP(PU2) or without RAMP-UP(PU1) :
a. Command timing reference Fig. 15 Power-Up command timing.
b. PU1 : will power-up the chip and set the VOUT to center value immediately and stay there.
c. PU2 : will power-up the chip and ramp-up COUT from bottom to center value and stay there.

(4). Power-down with RAMP-DOWN(PD2) or without RAMP-DOWN (PD1) :
a. Command timing reference Fig. 16 Power-Down command timing.
b. PDN1 will power-down the chip and set the VOUT data to bottom value immediately.
PDN1 will be executed correctly only if PU1 is executed before.
c. PDN2 will power-down the chip and ramp-down the COUT from its current to bottom value.
PDN2 will be executed correctly only if PU2 is executed before.

(5). Volume Set (VOL[3:0]) :
a. Command timing reference Fig.14 I2C Command timing.
b. D3 to D0 total 4bits(0 ~ 15) set volume level (max : 0, min : 15)

(6). Volume - - (VOL--) :
a. Command timing reference Fig.14 I2C Command timing.
b. Set volume level decrease.

(7). Volume + + (VOL++) :
a. Command timing reference Fig.14 I2C Command timing.
b. Set volume level increase.

(8). Pause and Resume (PAUSE; RESUME) :
a. Command timing reference Fig.14 I2C Command timing.
b. In Pause state, VOUT1 and VOUT2 will stay at logic LOW while the COUT will stay at the current D/A data level. When Resume, the COUT data will continue at the current D/A data level.

(9). Rewind :
a. Command timing reference Fig.14 I2C Command timing.
b. Play the current Voice Group from it is beginning.

- **MP3 Mode :**

This trigger mode is specially designed for simple MP3 function.

User can start to Play or Pause the voice by SBT pin, and Forward play by S2 pin, up to 1024 Voice Sections.

- SBT acts as (play/pause) or (play/stop).
- S2 act as forward.
- S3 acts as stop.

▪ BLOCK DIAGRAM :

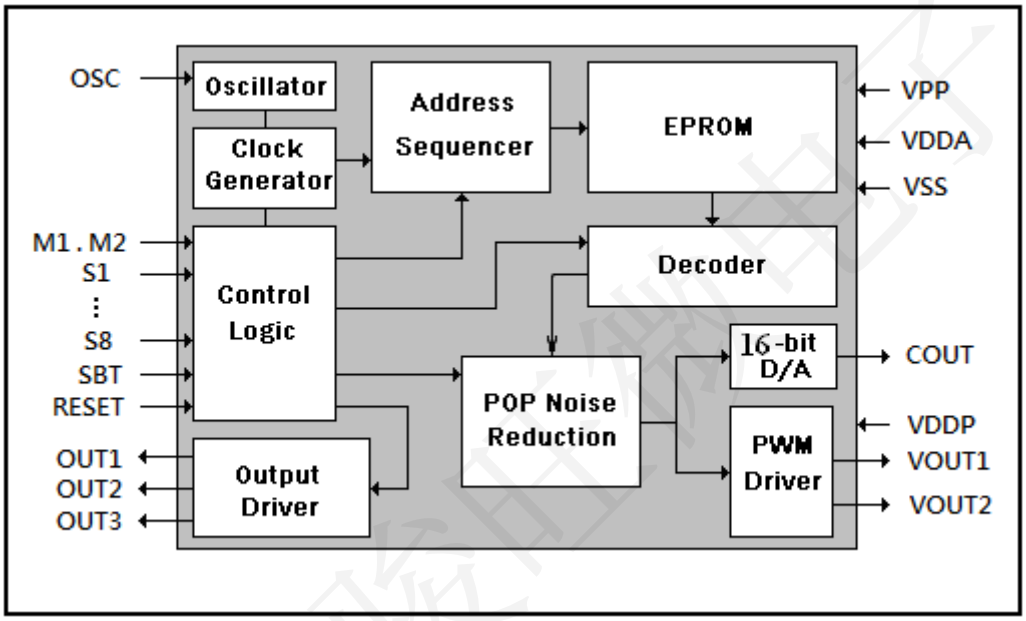


Fig. 17 Block Diagram

▪ ABSOLUTE MAXIMUM RATINGS :

Symbol	Rating	Unit
V_{DD} - V_{SS}	-0.5 ~ +5.0	V
V_{IN}	V_{SS} - 0.3 < V_{IN} < V_{DD} + 0.3	V
V_{OUT}	V_{SS} < V_{OUT} < V_{DD}	V
T (Operating):	-10 ~ +85	℃
T (Junction)	-10 ~ +85	℃
T (Storage)	-10 ~ +85	℃

DC CHARACTERISTICS (T_A = 0 to 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating Voltage	2.0		5.0	V	
ΔFc/Fc	Chip to chip frequency variation	-1.5		+1.5	%	

Symbol	Parameter	VDD	Min.	Typ.	Max.	Unit	Condition
I_{SB}	Standby current	3.3			1.0	uA	
		4.5			1.0		
I_{OP}	Operating current	3.3		11		mA	
		4.5		18			
I_{IH}	Input current	3.3		7		uA	V_{IL}=3.3V
		4.5		17			V_{IL}=4.5V
V_{IH}	Input high voltage	3.3		2/3 VDD		V	
		4.5					
V_{IL}	Input low voltage	3.3		1/3 VDD		V	
		4.5					
I_{OH}	Output high current	3.3		-16		mA	V_{OH}=2.0V
		4.5		-25			V_{OH}=3.5V
I_{OL}	Output low current	3.3		26		mA	V_{OL}=1.0V
		4.5		36			
I_{VOUT}	VOUT Current	3.3		150		mA	Load=8Ω
		4.5		220			
I_{COUT}	COUT Current	3.3		4		mA	V_{COUT}=1.0V full scale
		4.5		4			
ΔF/F	Frequency Stability	3.3		1.5		%	Note1
		4.5		1.5			Note2

Note1:

$$\frac{Fosc(3.3) - Fosc(2.7)}{Fosc(3.3)}$$

Note2:

$$\frac{Fosc(5.0) - Fosc(4.5)}{Fosc(4.5)}$$

▪ TIMING WAVEFORMS :

- KEY 、SBT and MP3 Trigger Mode :

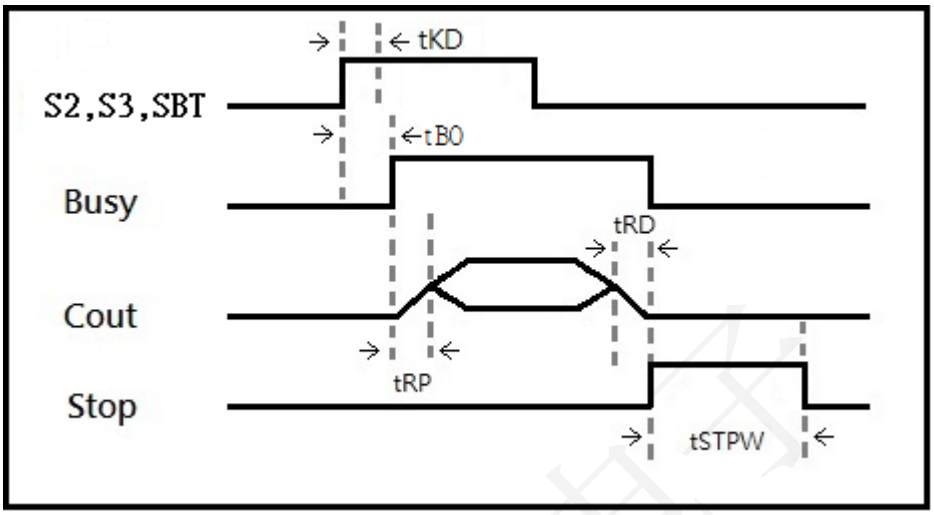


Fig. 18

- SPI Mode :

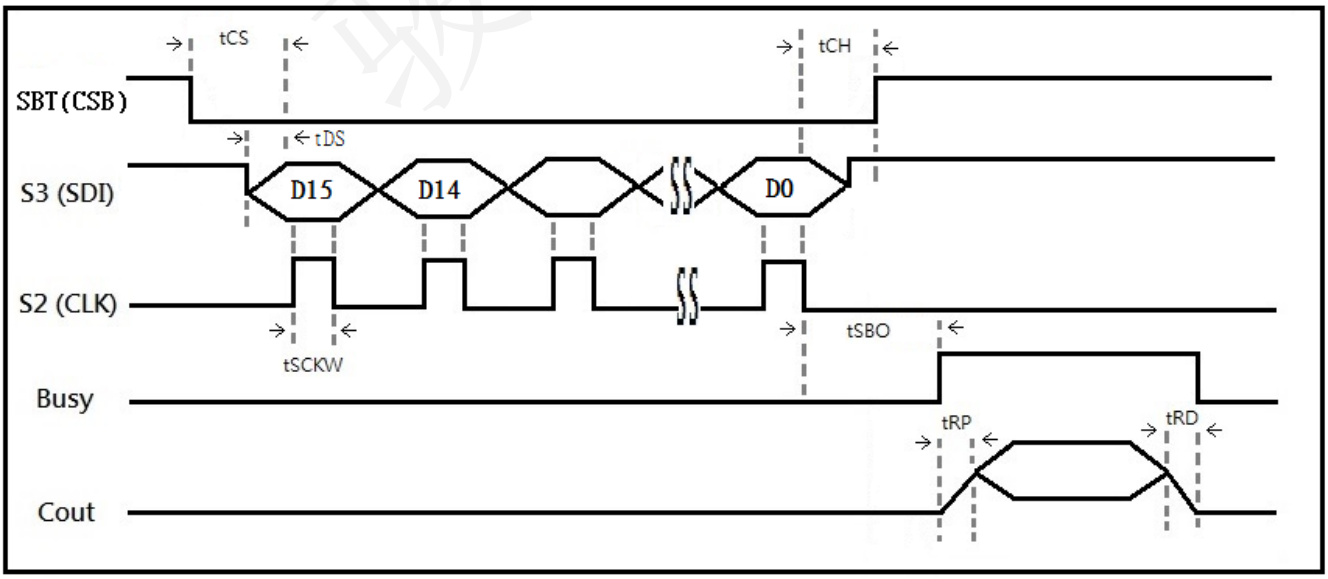


Fig. 19

- I2C Mode :

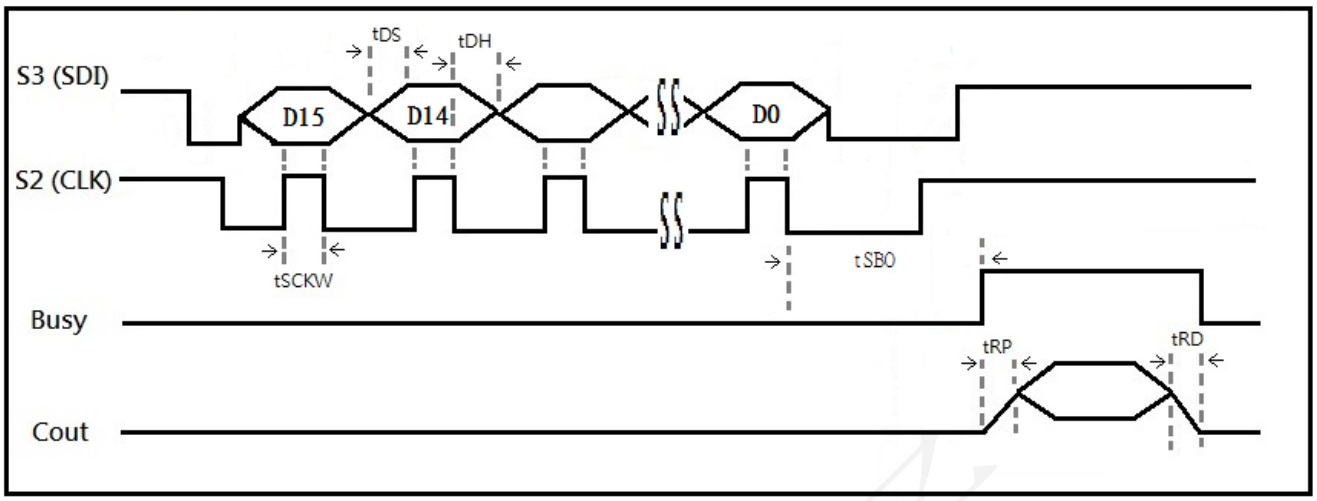


Fig. 20

▪ AC CHARACTERISTICS (T_A = 0 to 70℃, V_{DD} = 3.3V, V_{SS} = 0V, 8KHz sampling)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
t_{KD}	Key trigger debounce time (long)	—	16	—	ms	1
t_{KD}	Key trigger debounce time (long) – Retrigger during voice playback.	—	24	—	ms	1
t_{KD}	Key trigger debounce time (short)	—	1	—	ms	1
t_{KD}	Key trigger debounce time (short) – Retrigger during voice playback.	—	1.5	—	ms	1
t_{STPW}	STOP pulse width (long)	—	128	—	ms	1
t_{STPW}	STOP pulse width (short)	—	500	—	μs	1
t_{AS}	Address set-up time	300	—	—	ns	
t_{AH}	Address hold time	300	—	—	ns	
t_{SBTW}	SBT stroke pulse width (long)	16	—	—	ms	1
t_{SBTW}	SBT stroke pulse width (short)	1	—	—	ms	1
t_{BO}	BUSY signal output delay time(long)	—	24	—	ms	1
t_{BO}	BUSY signal output delay time(short)	—	1	—	ms	1
t_{CS}	Chip select set-up time	100	—	—	ns	
t_{CH}	Chip select hold time	100	—	—	ns	
t_{SCKW}	Serial clock pulse width	1	—	—	μs	
t_{DS}	Data set-up time	100	—	—	ns	
t_{DH}	Data hold time	100	—	—	ns	
t_{SBO}	BUSY signal output delay time	—	—	2	ms	
t_{RP}	Ramp Up time	—	160	—	ms	
t_{RD}	Ramp Down time	—	160	—	ms	
t_{FD}	Full signal output delay time	—	—	2	ms	

Notes :

The long or short debounce time is selectable as whole chip option during Voice Files Compiling.

In Circuit Program Applications ：

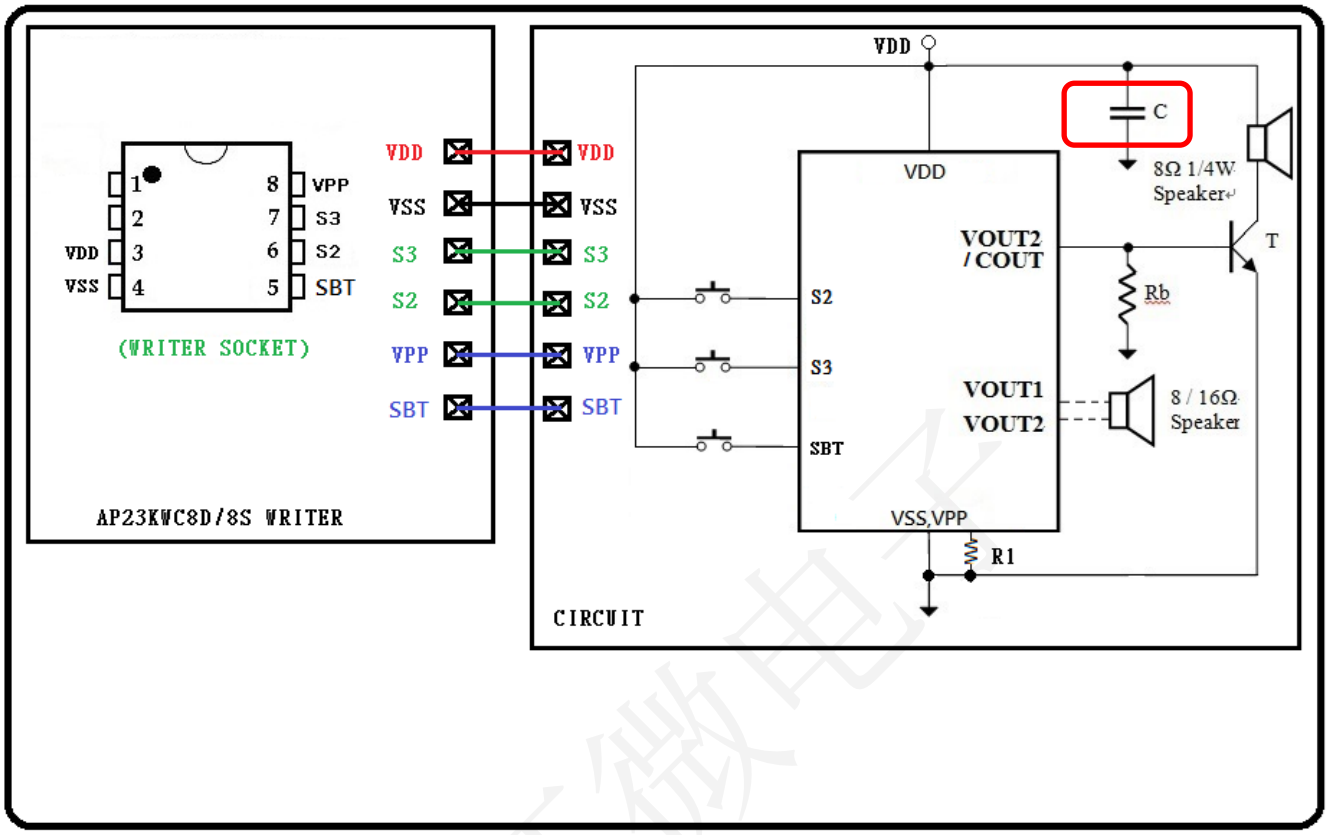


Fig. 21

1. Between VPP and GND should add R1(10K)Ω.
2. Between Writer and Circuit connect wire less than 10cm is the better.
3. If voltage is higher than 4.0V, C (0.1uF(typ)) is necessary for endure high voltage and protect it from noise which may affect its performance
   Distance between caps and ICs should be minimized to reduce spreading inductance.
   The wiring length between the IC and caps may be less than 100mil.

▪ TYPICAL APPLICATIONS ：

Key Mode

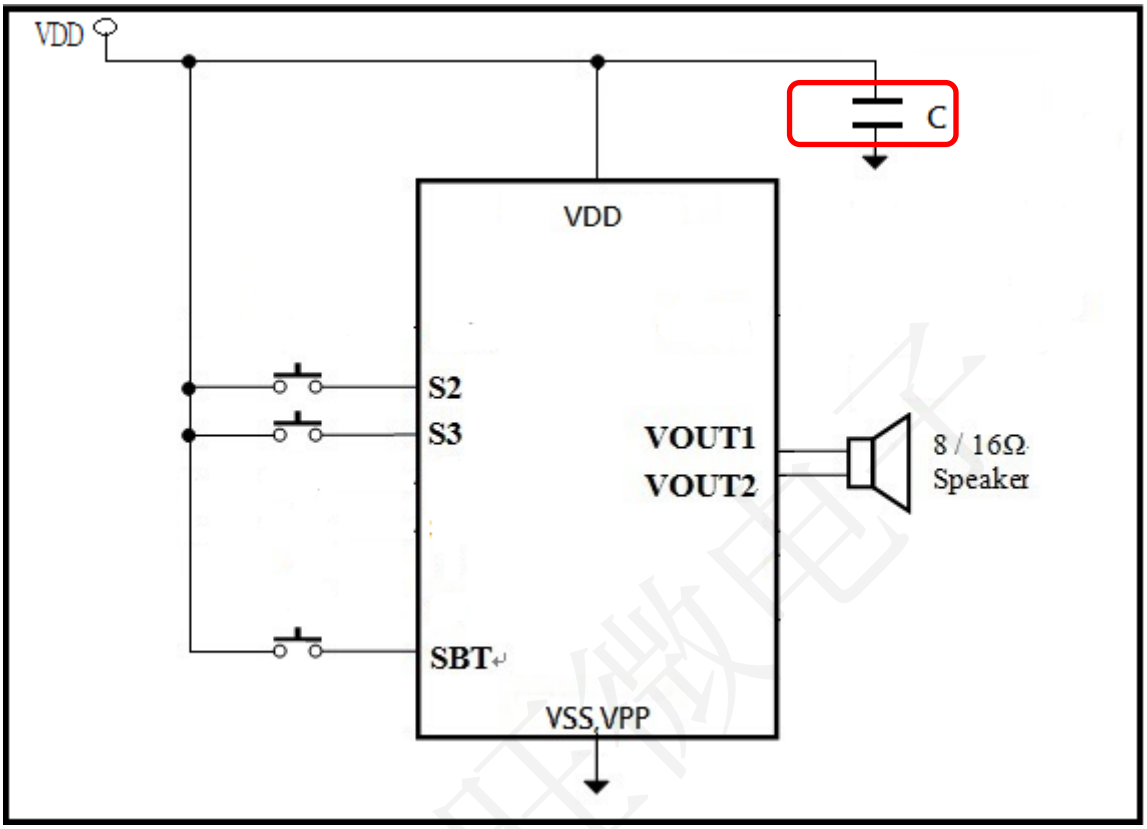


Fig.22

Note:

If voltage is higher than 4.0V, C (0.1uF$_{(typ)}$) is necessary for endure high voltage and protect it from noise which may affect its performance

Distance between caps and ICs should be minimized to reduce spreading inductance.

The wiring length between the IC and caps may be less than 100mil.

SPI Mode

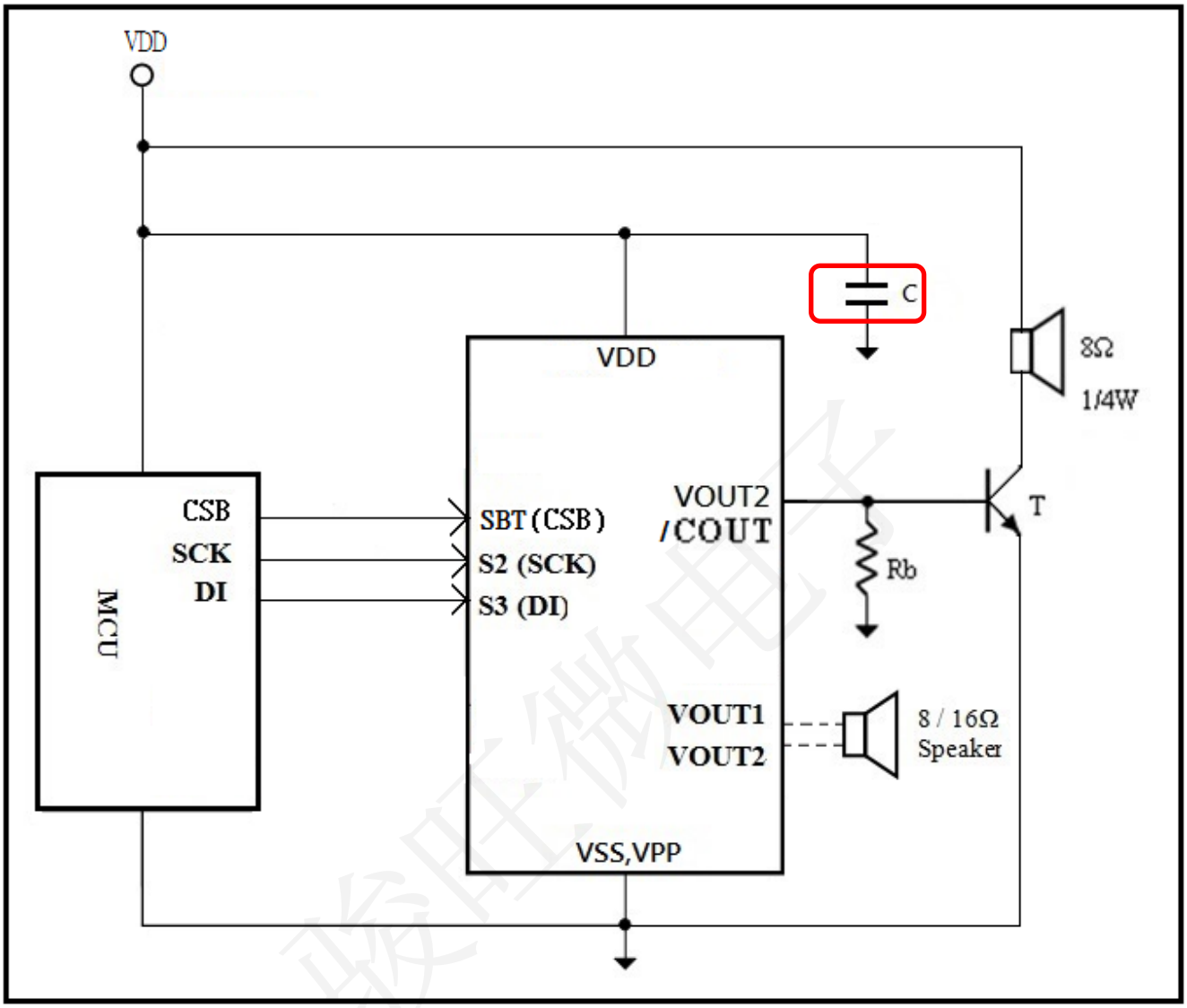


Fig. 23

Note:

If voltage is higher than 4.0V, C (0.1uF$_{(typ)}$) is necessary for endure high voltage and protect it from noise which may affect its performance

Distance between caps and ICs should be minimized to reduce spreading inductance.

The wiring length between the IC and caps may be less than 100mil.

I2C Mode

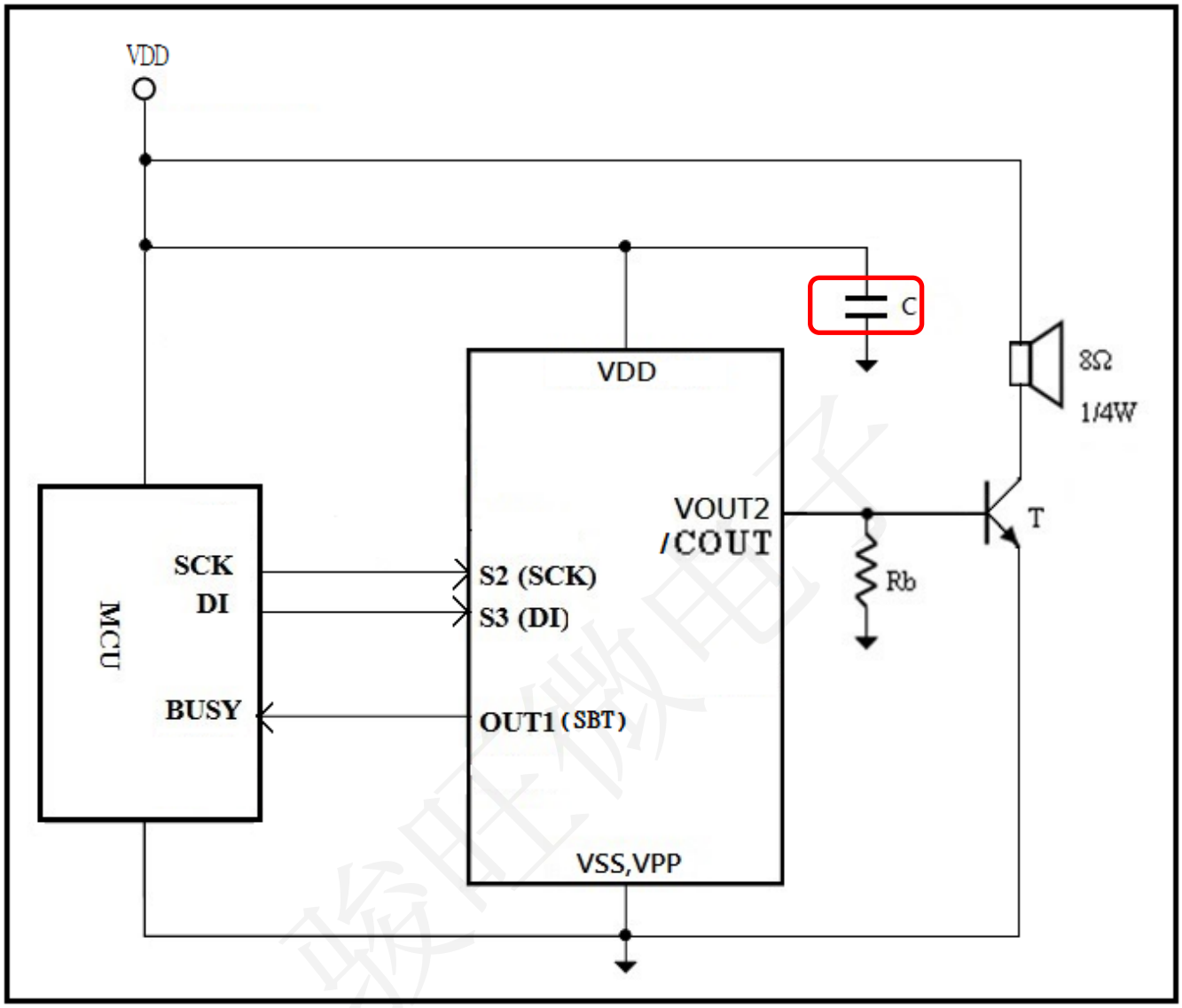


Fig. 24

Note:

If voltage is higher than 4.0V, C (0.1uF$_{(typ)}$) is necessary for endure high voltage and protect it from noise which may affect its performance

Distance between caps and ICs should be minimized to reduce spreading inductance.

The wiring length between the IC and caps may be less than 100mil.

MP3 Mode

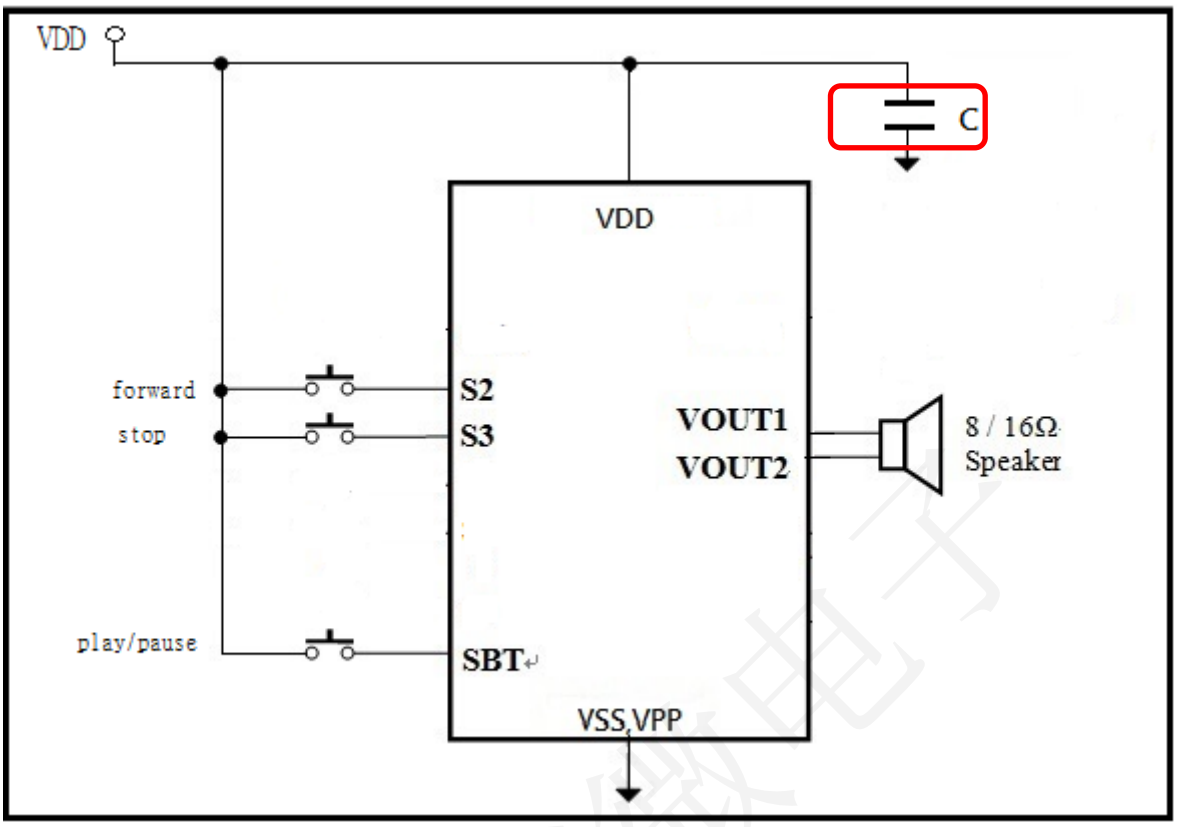


Fig. 25

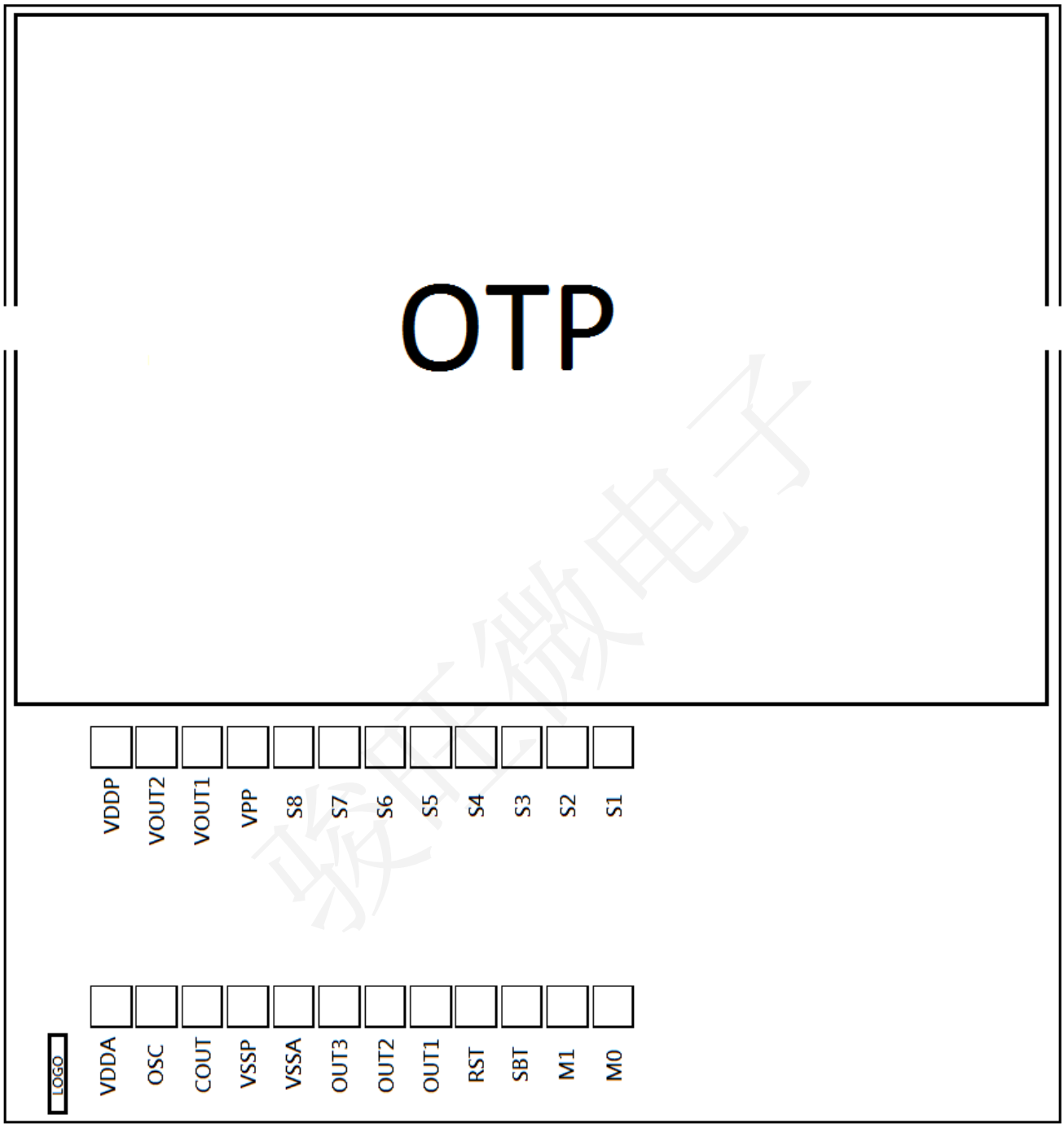
Note:

If voltage is higher than 4.0V, C (0.1uF(typ)) is necessary for endure high voltage and protect it from noise which may affect its performance

Distance between caps and ICs should be minimized to reduce spreading inductance.

The wiring length between the IC and caps may be less than 100mil.

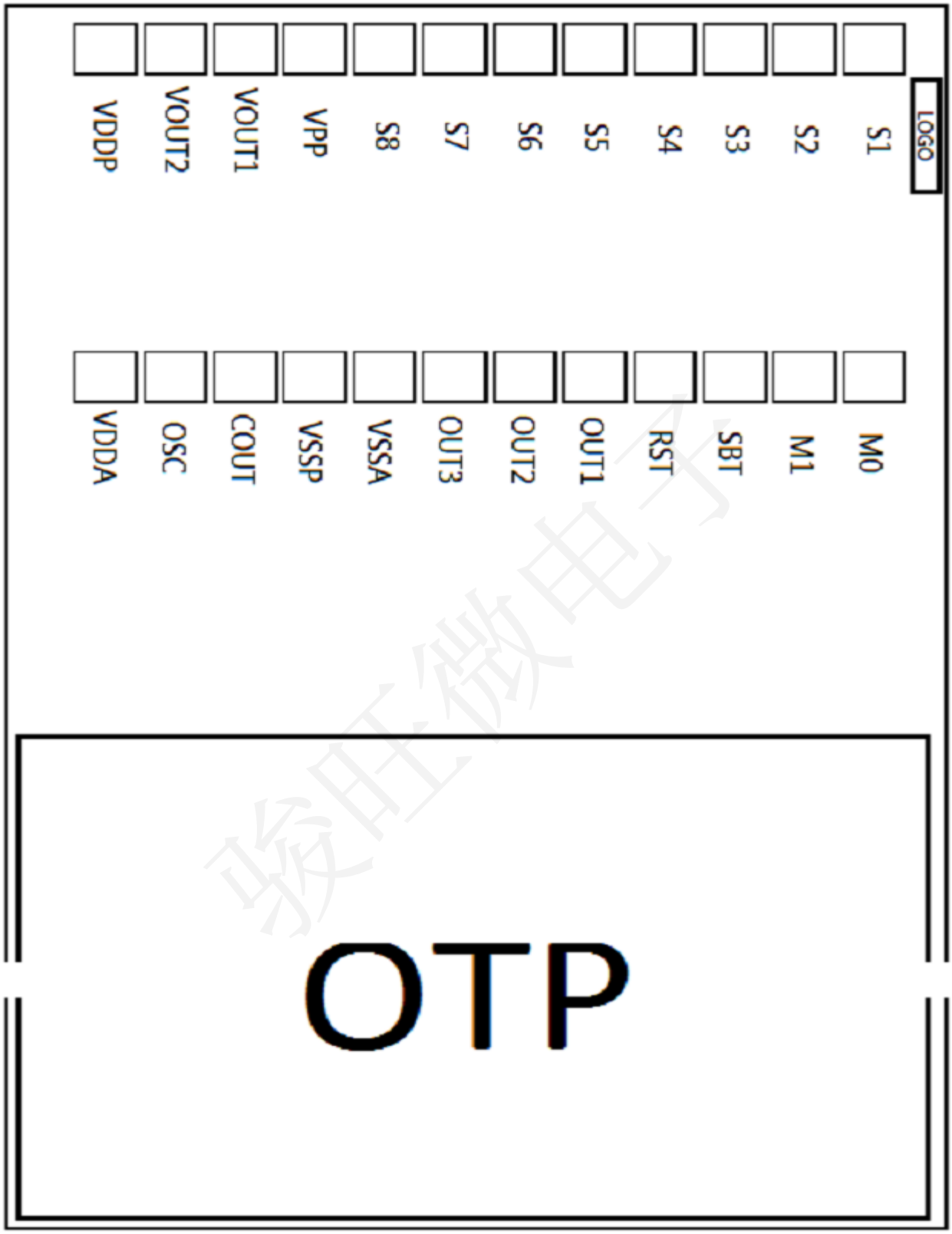
- **BONDING PAD DIAGRAMS (aP23682/aP23341)**



Notes:

1. Between VPP and GND should add 10KΩ.
2. VDDA and VDDP should be connected to the Positive Power Supply.
3. VSSA and VSSP should be connected to the Power GND.
4. Substrate should be connected to the Power GND.

BONDING PAD DIAGRAMS (aP23170/aP23085)

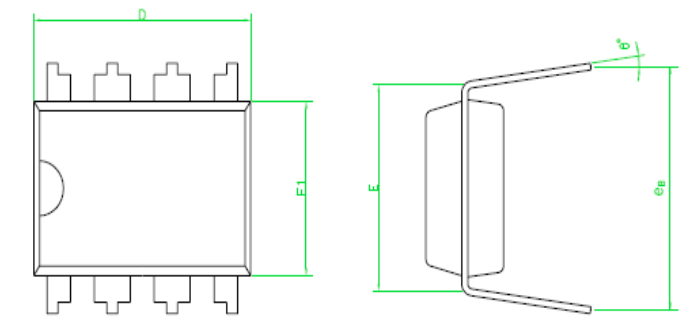


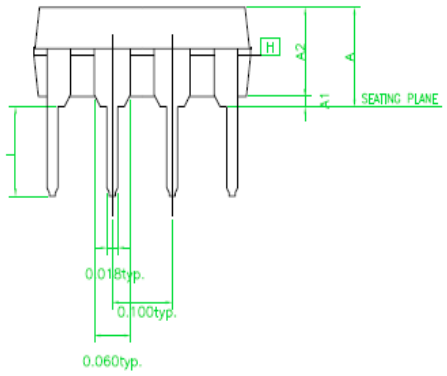
Notes:

1.Between VPP and GND should add 10KΩ.
2.VDDA and VDDP should be connected to the Positive Power Supply.
3.VSSA and VSSP should be connected to the Power GND.
4.Substrate should be connected to the Power GND.

PACKAGES DIMENSION OUTLINES

8-Pin 300mil P-DIP Package





SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:

1.JEDEC OUTLINE : MS-001 BA

2."D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.

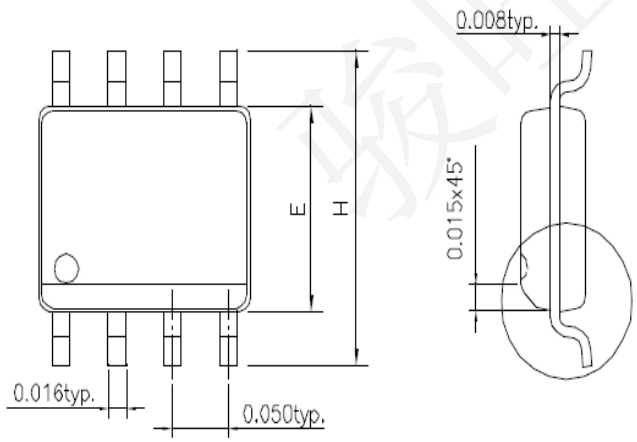
3.eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.

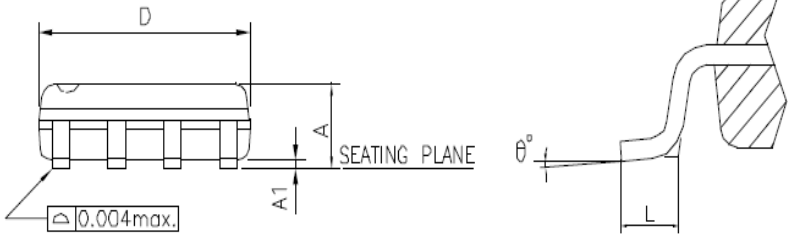
4.POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.

5.DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.

6.DATUM PLANE H COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

8-Pin 150mil SOP Package





SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:

1.JEDEC OUTLINE : MS-012 AA

2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.

3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

HISTORY

2015/07/20

aP23682_341__170_085 SPEC : Modify cpu control timing waveforms
Modify Page. 15 DC CHARACTERISTICS
Reduce output function from 14 to 9.

2015/09/08

aP23682_341__170_085 SPEC : Modify ULAW5 to ULAW8.
Add SBT mode independent description.
Optimize the CPU mode control.
Add In Circuit Program application on page. 22.

2015/12/23

aP23682_341__170_085 SPEC : Add decoupling cap suggestion at high voltage application.
Page 22 to 26.

2016/05/24

aP23682_341__170_085 SPEC : Modify in circuit program schematic to support copier.
Page 3,22.